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BRIGHTON

CPU : VIA ISAIAH
Chip Set : VIA VX800
Remarks :

Model Name : BRIGHTON MAIN

PCB Part No :

Dev. Step : PV

Revision : 1.0

T.R. Date : 2008.11.07

DRAW	CHECK	APPROVAL

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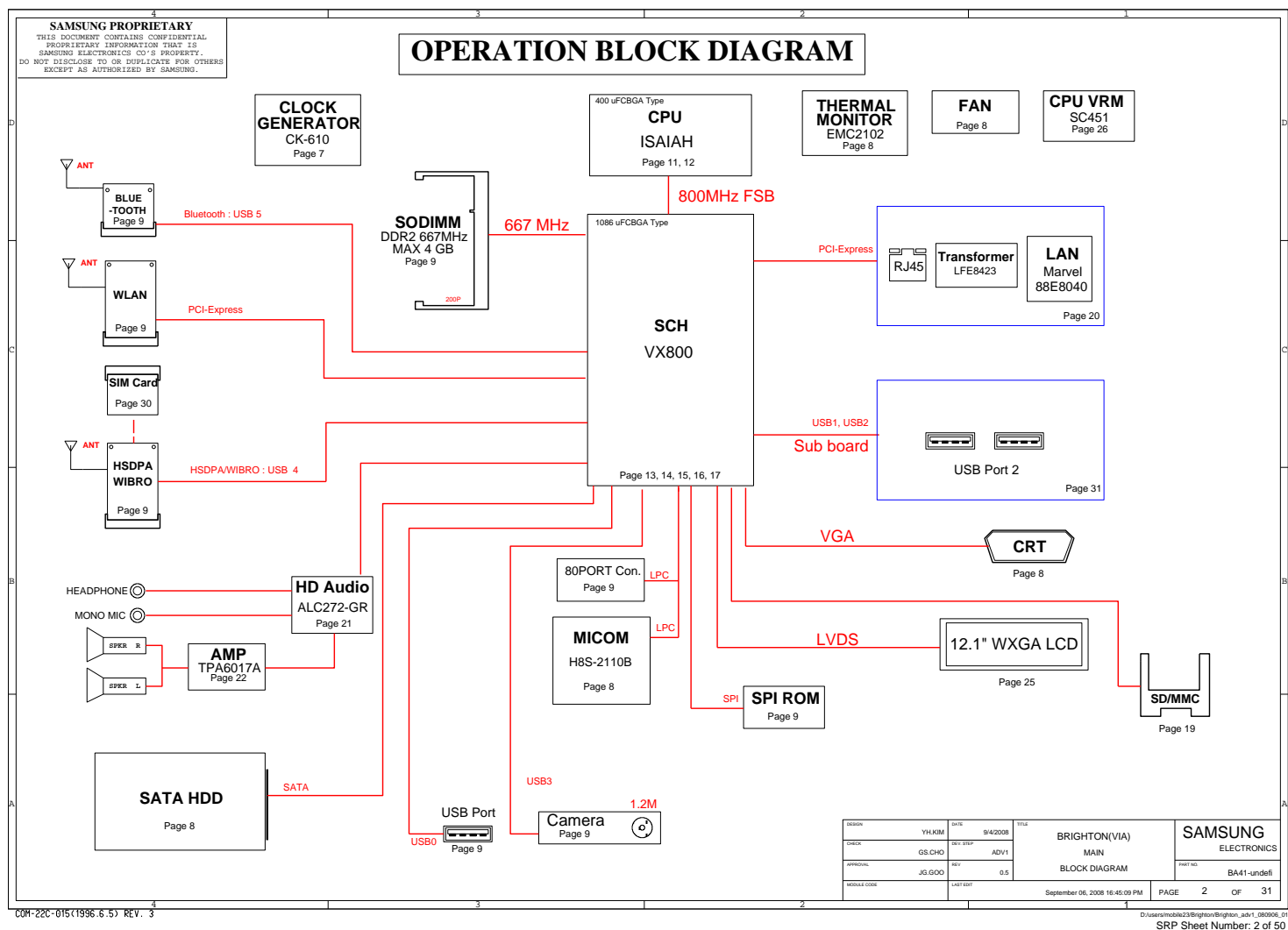
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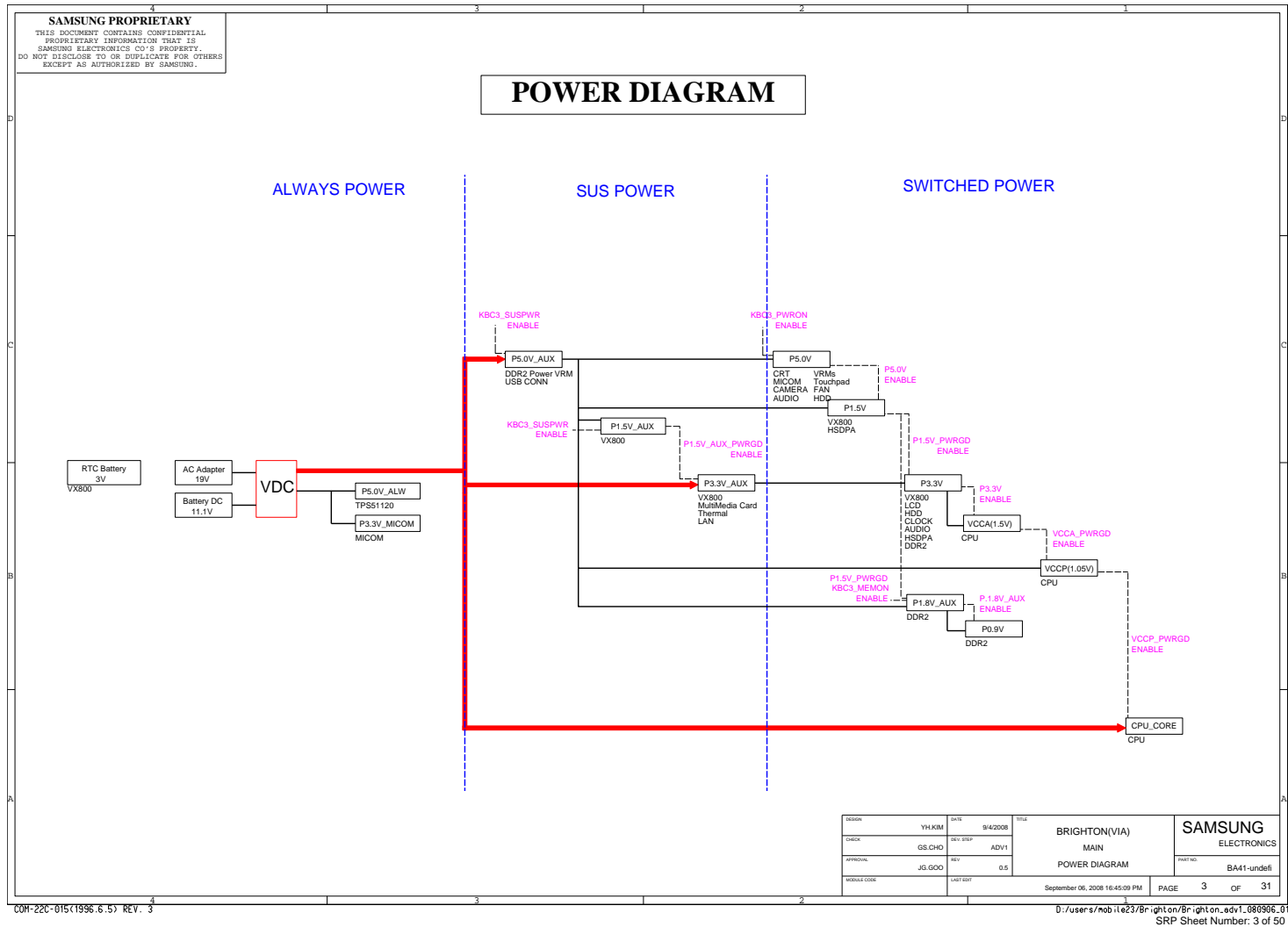
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DESIGN	YHKIM	DATE	9/4/2008	TITLE	BRIGHTON(VIA)	SAMSUNG
CHECK	GS.CHO	DEV. STEP	ADV1	MAIN		ELECTRONICS
APPROVAL	JG.GOO	REV	0.5	COVER		PART NO.
MODULE CODE		LAST EDIT				BA41-undefi
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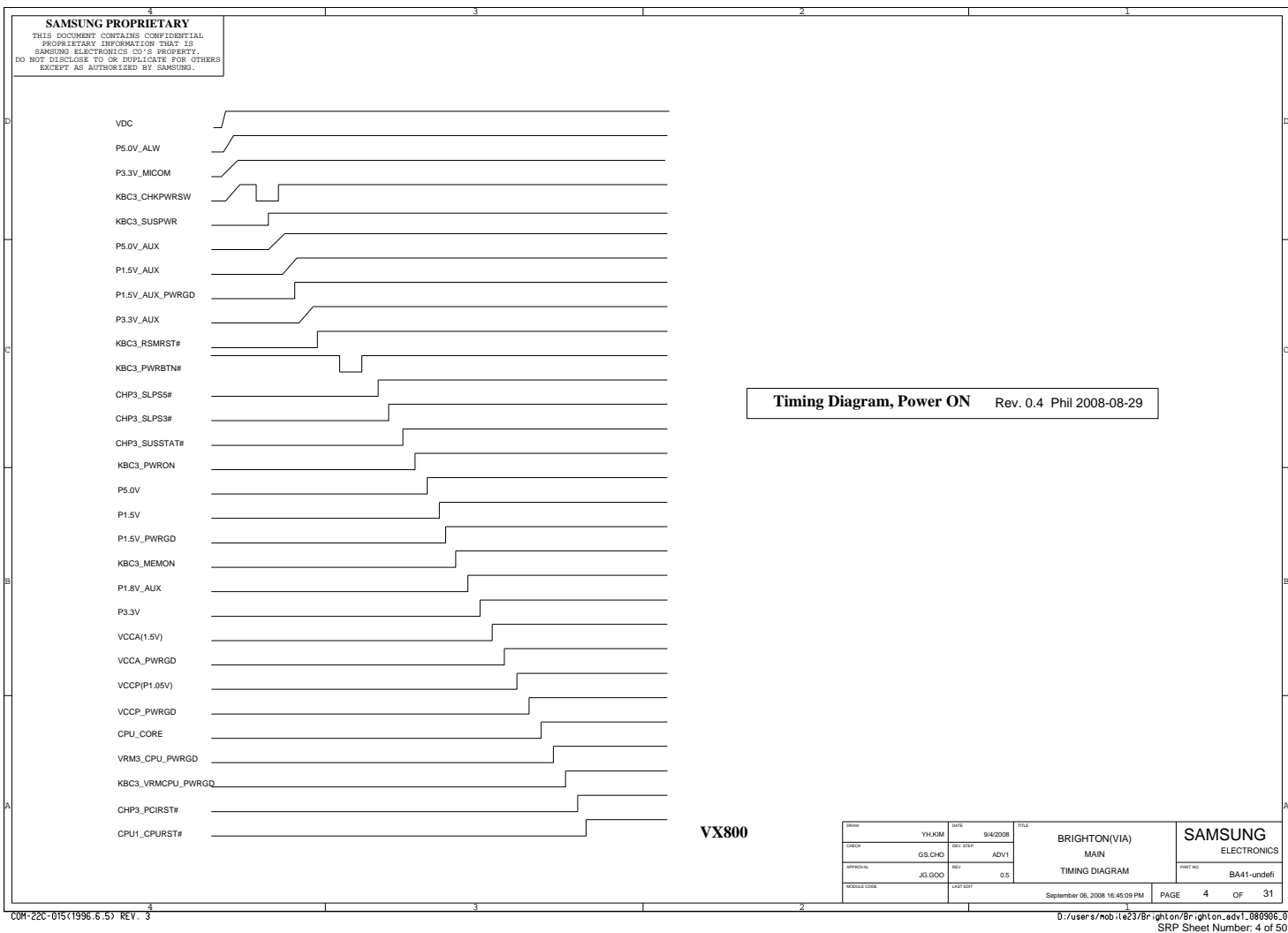
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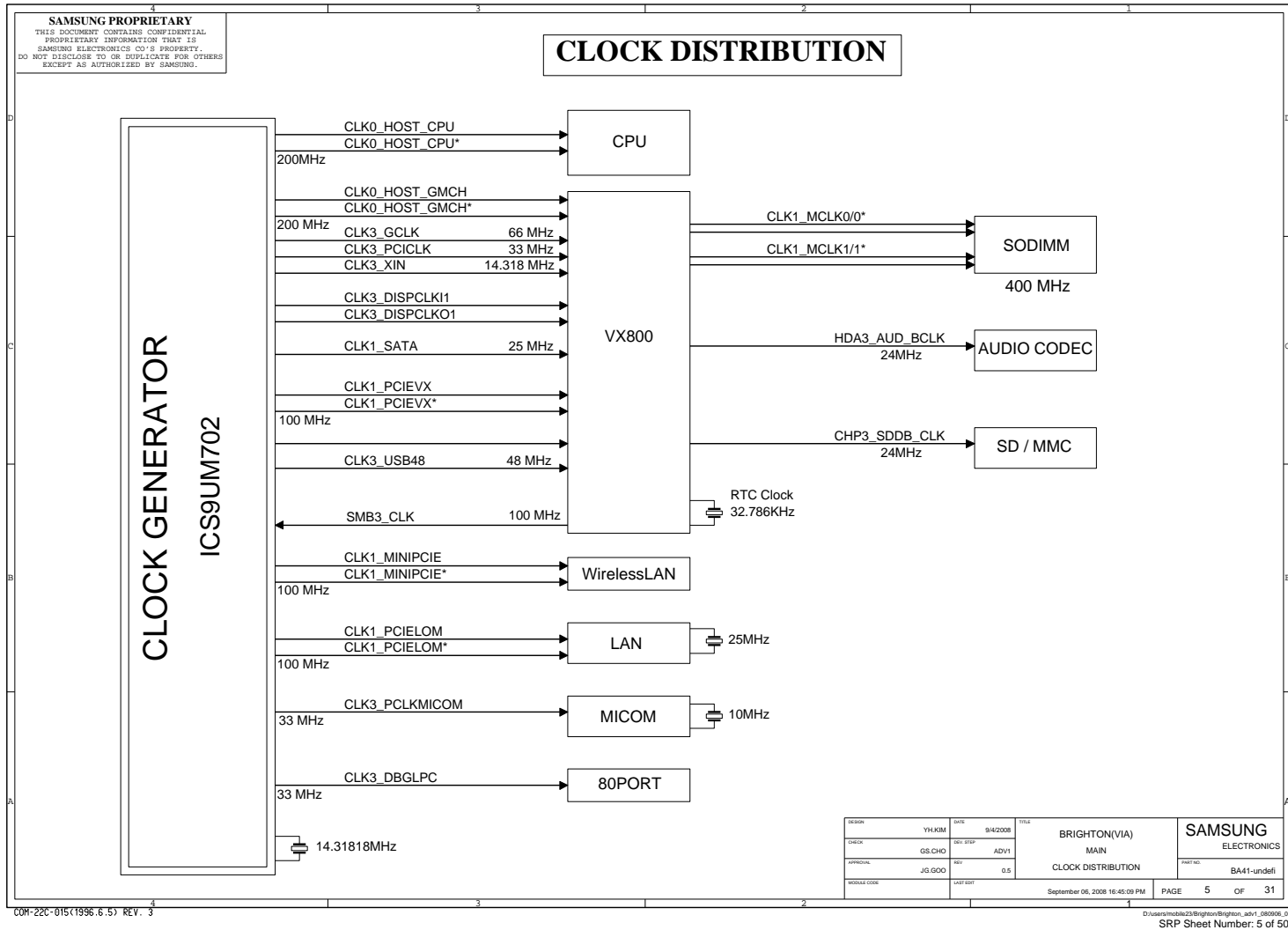
8. Block Diagram and Schematic



8. Block Diagram and Schematic



8. Block Diagram and Schematic



BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Wired LAN	AD21	3	G
USB	AD29(internal)	Programable	
Hub to PCI	AD30(internal)		
LPC Bridge/IDE/AC97/SMBUS	AD31(internal)		

I²C / SMB Address

Devices	Address	Hex	Bus
VX800	Master	-	SMBUS Master
ICS9UM702(Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
SODIMM0	1010 000X	A0h	
MICOM	Master	-	
BATTERY	0001 011h	16h	
THERMAL MORNITOR	x111 1010	7Ah	

USB PORT Assign

Port0	Main BD USB Port
Port1	SUB BD USB Port1
Port2	SUB BD USB Port2
Port3	Camera
Port4	HSDPA
Port5	Bluetooth

Voltage Rails

Power Rail	Descriptions
PRTC_BAT VDC	3.3V (can drop to 2.0V min. in G3 state) supply for the RTC well. Primary DC system power supply (6 to 19V)
PSV_AUX	5.0V power rail (off in S4-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P1.8V_AUX	GMCHDDR II Power Source(off in S4-S5)
P1.5V_AUX	GMCH Power Source(off in S4-S5)
PSV	5.0V switched power rail (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
VCCA(1.5V)	1.5V CPU power rail (off in S3-S5)
VCCP1.05V	1.05V CPU power rail (off in S3-S5)
CPU_CORE	Core voltage for VIA NANO CPU.
P3.3V_MICOM	3.3V always on power rail for MICOM
LCD_VDD3.3V	3.3V (LCD)
VCC_CRT	5V (CRT)
2.5V_LAN	2.5V(88E9040)
P4.75_AUD	4.75V (ALC272)
P5.0V_AUD	5V(ALC272)
P5.0V_AMP	5V (Audio AMP)

CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1	1.180 V
0	0	0	0	1	0	1.676 V	1	0	0	0	1	0	1.164 V
0	0	0	0	1	1	1.660 V	1	0	0	0	1	1	1.148 V
0	0	0	1	0	0	1.644 V	1	0	0	1	0	0	1.132 V
0	0	0	1	0	1	1.628 V	1	0	0	1	0	1	1.116 V
0	0	0	1	1	0	1.612 V	1	0	0	1	1	0	1.100 V
0	0	0	1	1	1	1.596 V	1	0	0	1	1	1	1.084 V
0	0	1	0	0	0	1.580 V	1	0	1	0	0	0	1.068 V
0	0	1	0	0	1	1.564 V	1	0	1	0	0	1	1.052 V
0	0	1	0	1	0	1.548 V	1	0	1	0	1	0	1.036 V
0	0	1	0	1	1	1.532 V	1	0	1	0	1	1	1.020 V
0	0	1	1	0	0	1.516 V	1	0	1	1	0	0	1.004 V
0	0	1	1	0	1	1.500 V	1	0	1	1	0	1	0.988 V
0	0	1	1	1	0	1.484 V	1	0	1	1	1	0	0.972 V
0	0	1	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V
0	1	0	0	0	0	1.452 V	1	1	0	0	0	0	0.940 V
0	1	0	0	0	1	1.436 V	1	1	0	0	0	1	0.924 V
0	1	0	0	1	0	1.420 V	1	1	0	0	1	0	0.908 V
0	1	0	0	1	1	1.404 V	1	1	0	0	1	1	0.892 V
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0	0.876 V
0	1	0	1	0	1	1.372 V	1	1	0	1	0	1	0.860 V
0	1	0	1	1	0	1.356 V	1	1	0	1	1	0	0.844 V
0	1	0	1	1	1	1.340 V	1	1	0	1	1	1	0.828 V
0	1	1	0	0	0	1.324 V	1	1	1	0	0	0	0.812 V
0	1	1	0	0	1	1.308 V	1	1	1	0	0	1	0.796 V
0	1	1	0	1	0	1.292 V	1	1	1	0	1	0	0.780 V
0	1	1	0	1	1	1.276 V	1	1	1	0	1	1	0.764 V
0	1	1	1	0	0	1.260 V	1	1	1	1	0	0	0.748 V
0	1	1	1	0	1	1.244 V	1	1	1	1	0	1	0.732 V
0	1	1	1	1	0	1.228 V	1	1	1	1	1	0	0.716 V
0	1	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V

DOTHAN-ULV Base Stealey

HIGH FREQUENCY MODE

DOTHAN-ULV Base Stealey

LOW FREQUENCY MODE

DOTHAN-ULV Base Stealey

DEEPER SLEEP MODE

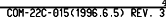
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APPROVAL	JG-GOO	REV	0.5		BOARD INFORMATION	PART NO. BA41-undefi
WORKS CODE	JST 021					
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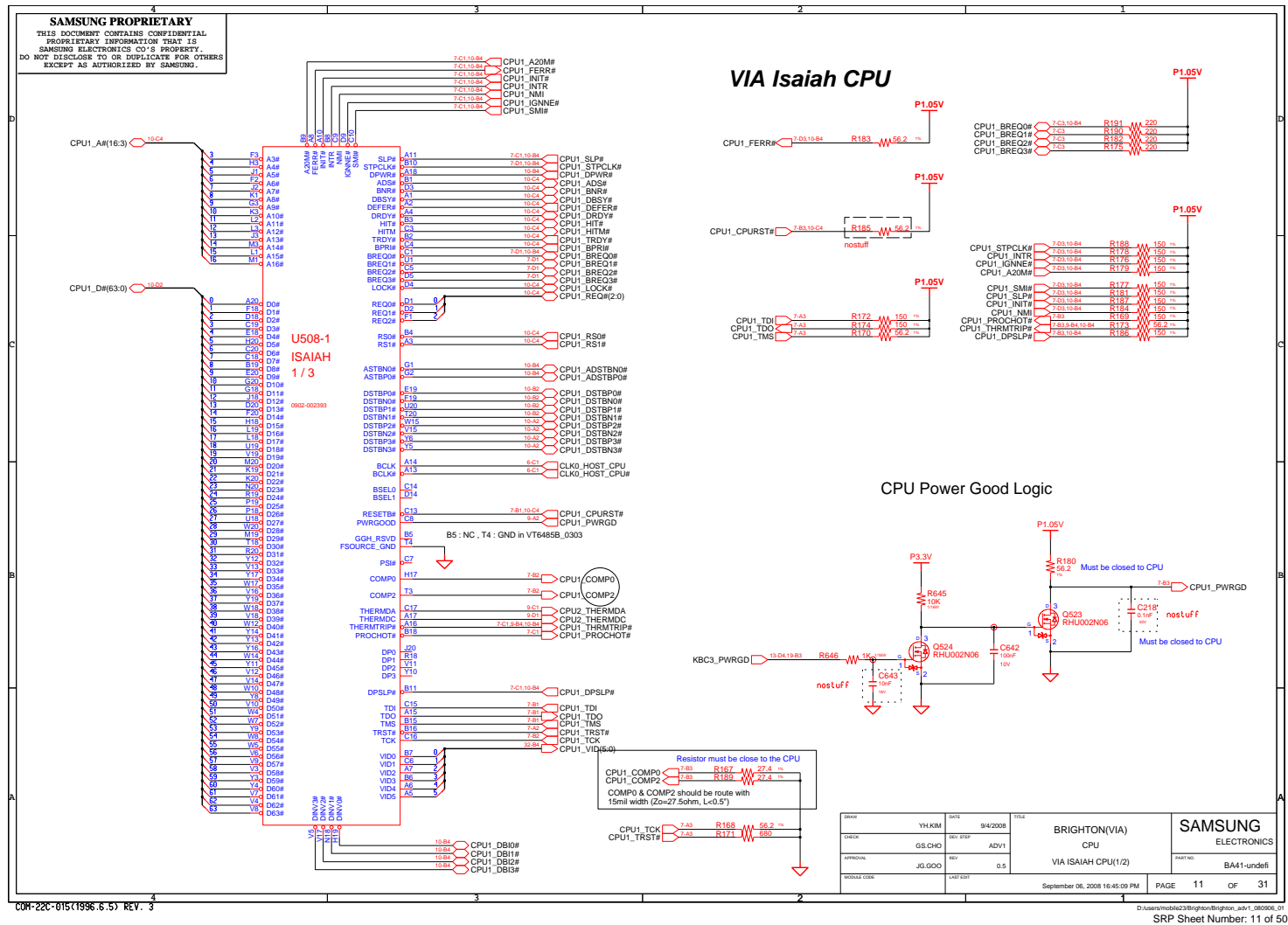
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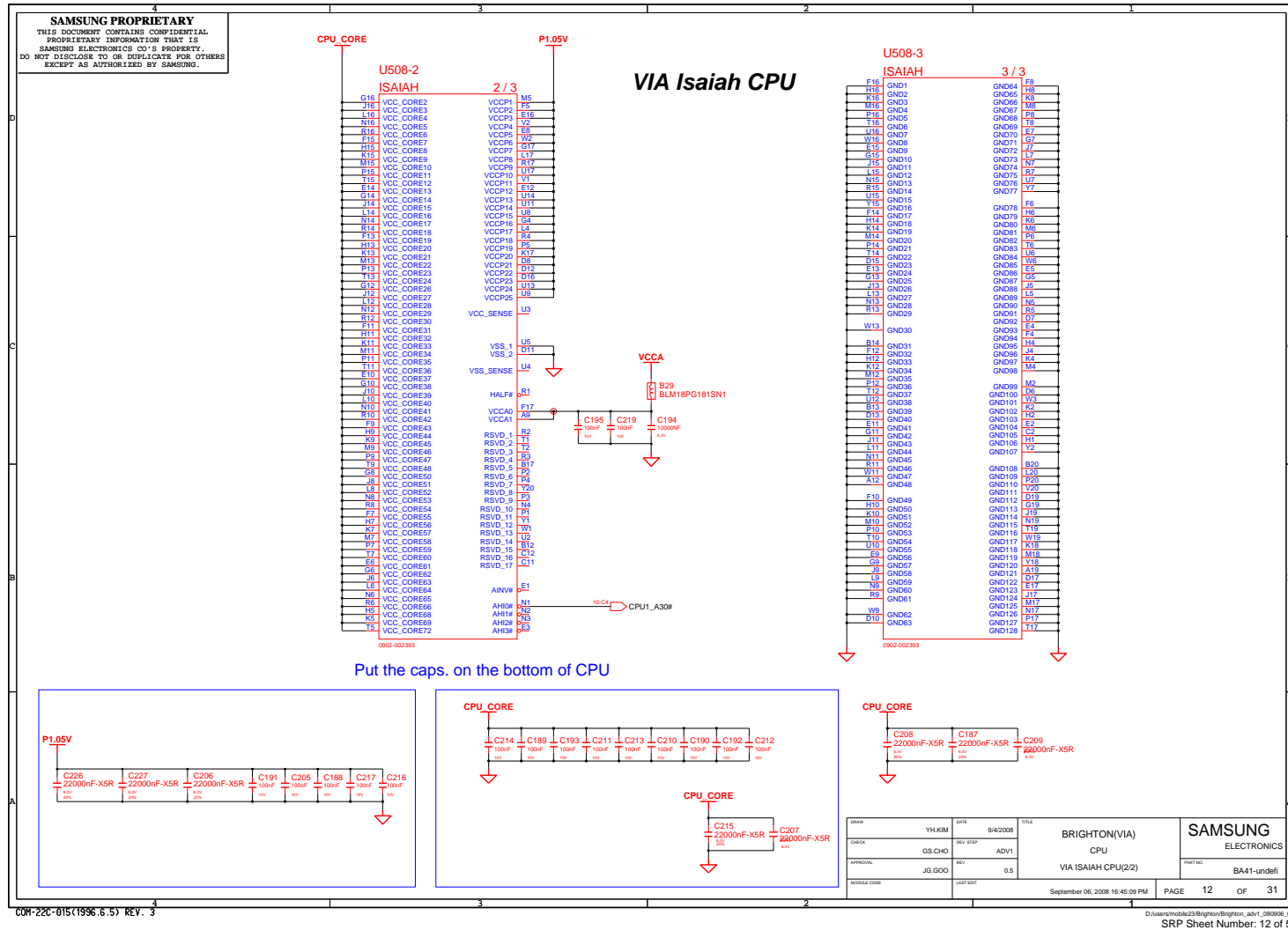
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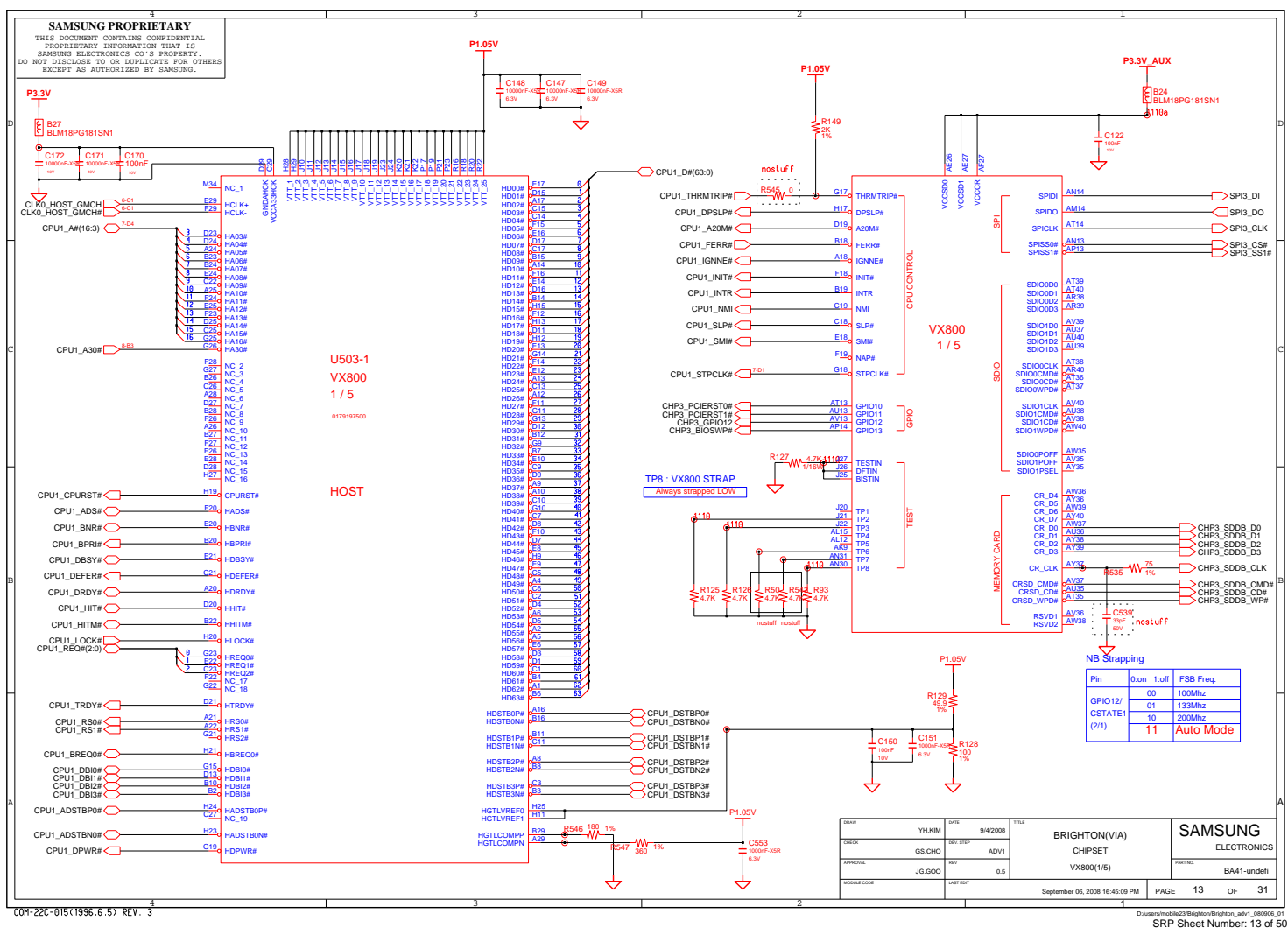
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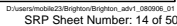
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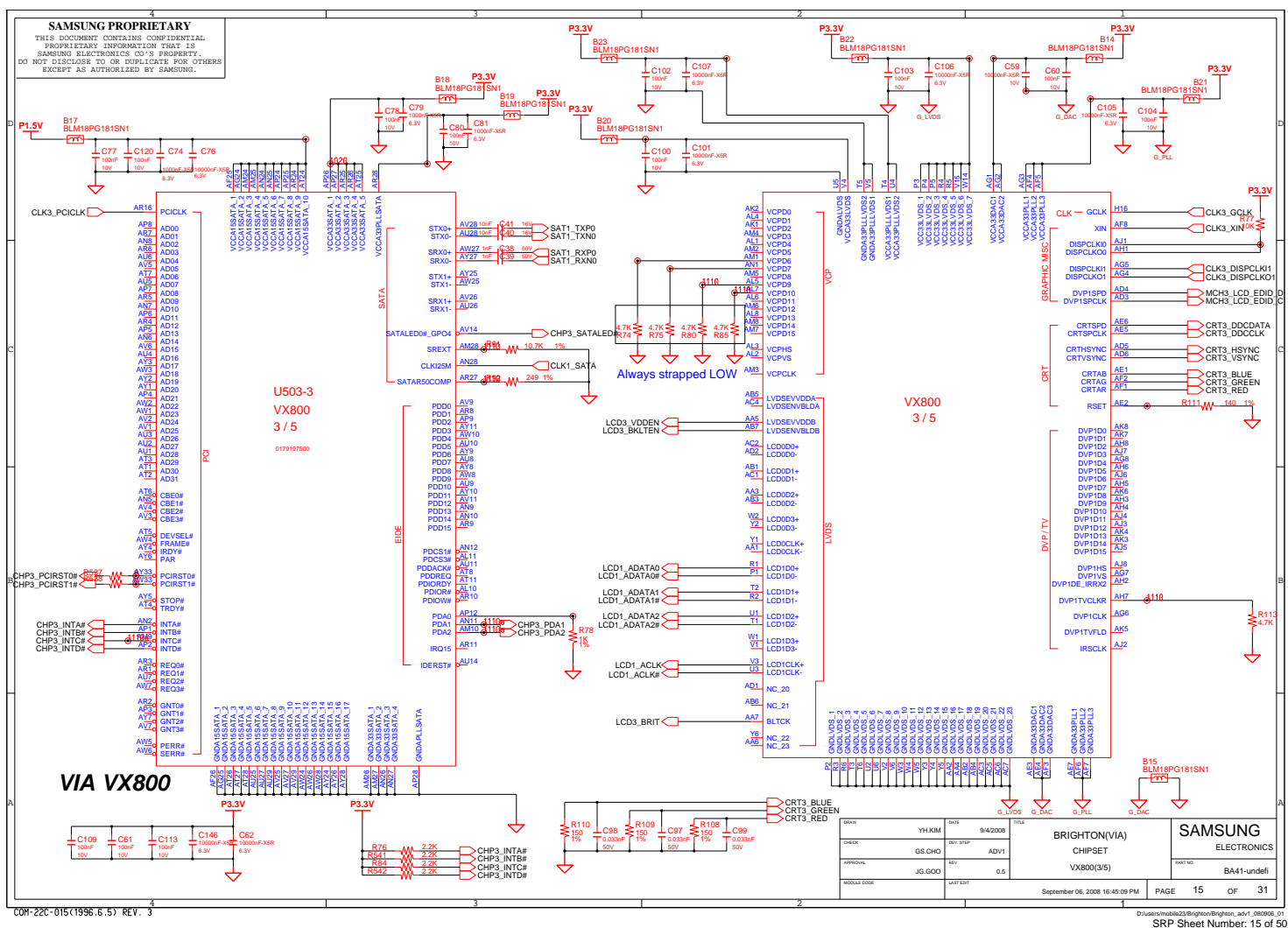
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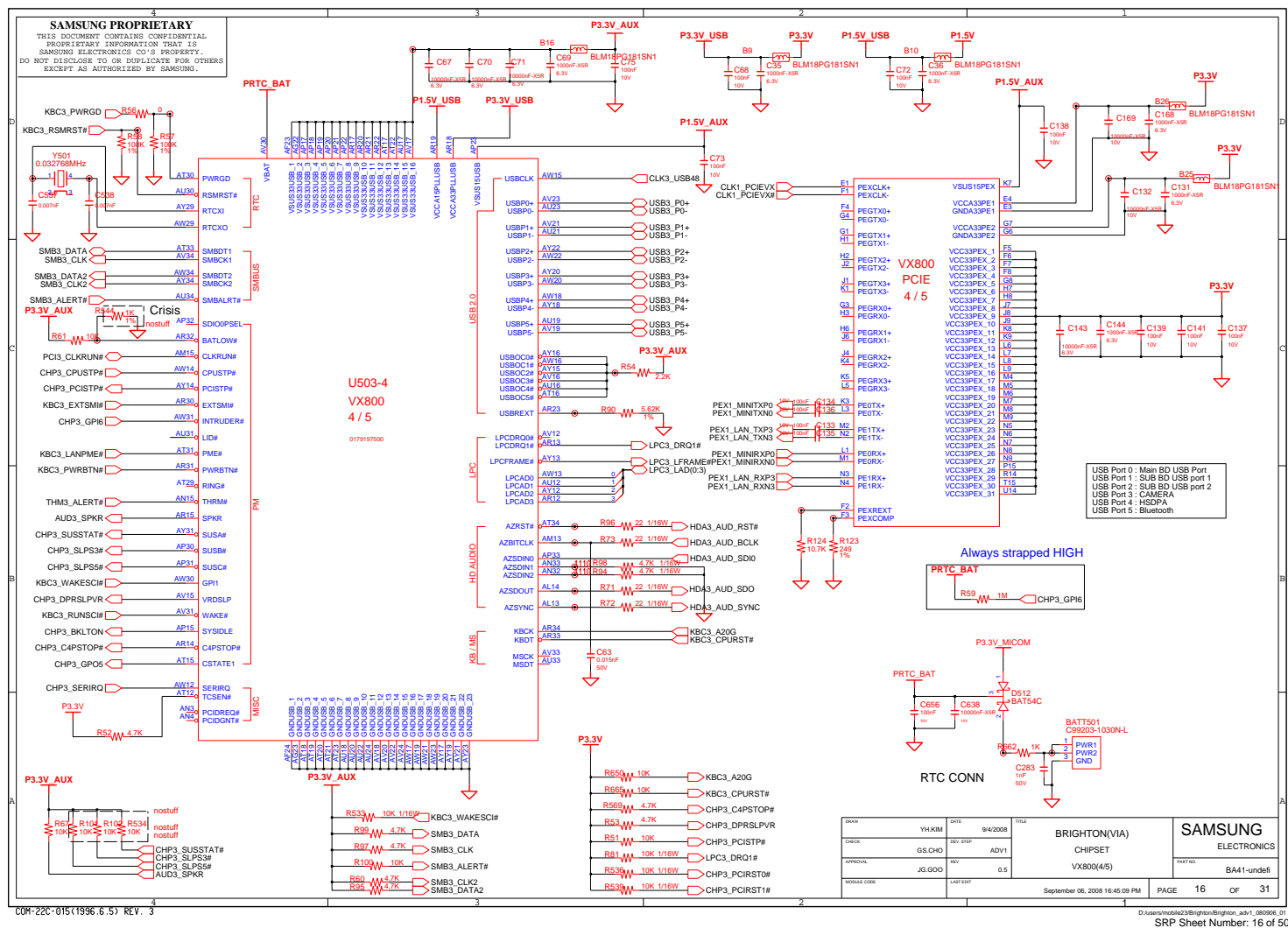
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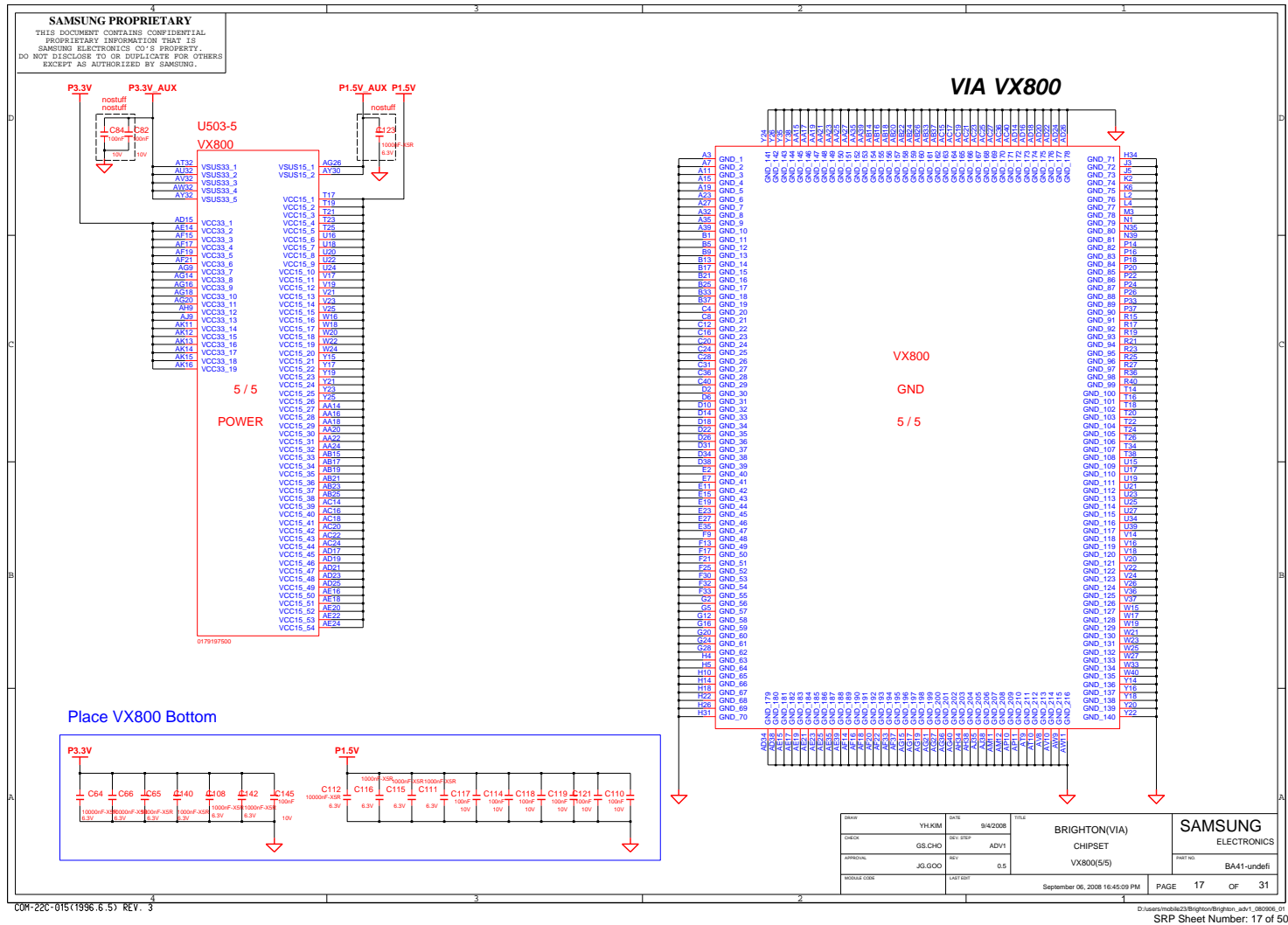
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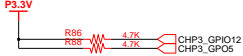
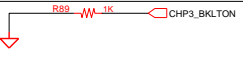
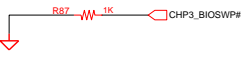
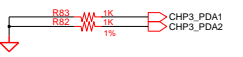
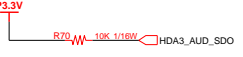

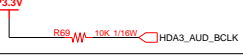
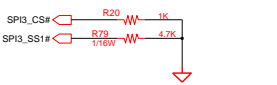
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8. Block Diagram and Schematic



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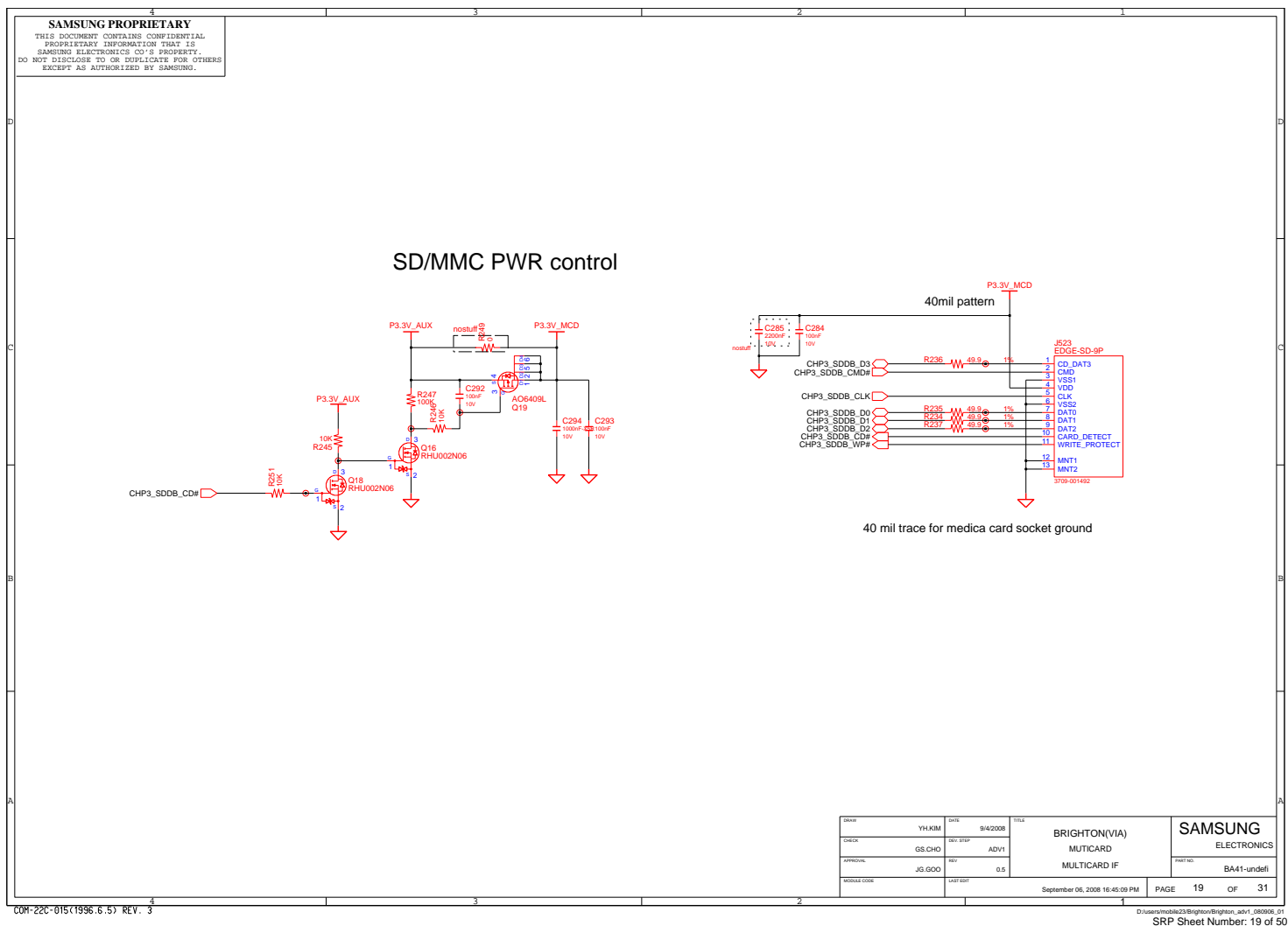
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Signal	Ball#	Function	Description	
	GPIO12	AV13	FSB Clock	State(GPIO12 : CSTATE1) Mode(MHz)
	CSTATE1	AT15	AT15	LL 100MHz
				LH 133MHz
				HL 200MHz
				HH Auto
	SYSIDLE	AP15	IO Queue Depth	L : 12-level deep H : 1-level deep
	GPIO13	AP14	GTL Pull-up	L : Enable internal GTL Pull-up H : Disable internal GTL Pull-up
	PDA1	AN11	Dual Processor Configuration	L : Single Processor H : Dual Processor
	PDA2	AM10	PLL_OK Source Selection	L : PLL_OK from PLL H : PLL_OK_from logic counter
	AZSDOUT	AL14	Auto Reboot	L : Enable H : Disable
	AZSYNC	AL13	LPC FWH Command	L : Enable H : Disable
	AZBITCLK	AM13	SPI/LPC ROM Select	L : LPC ROM H : SPI ROM
	SPISS[1:0]#	AP13 AN13	IDE Controller [sata table support]	State(SPISS[1:0]#) Mode LL IDE Reserved

DRAW	YH.KIM	DATE	9/4/2008	TITLE	BRIGHTON(VIA)	SAMSUNG
CHECK	GS.CHO	REV. STEP	ADV1	CHIPSET		ELECTRONICS
APPROVAL	JG.GOO	REV.	0.5	VX800 STRAP		SHEET NO. BA41-undefi
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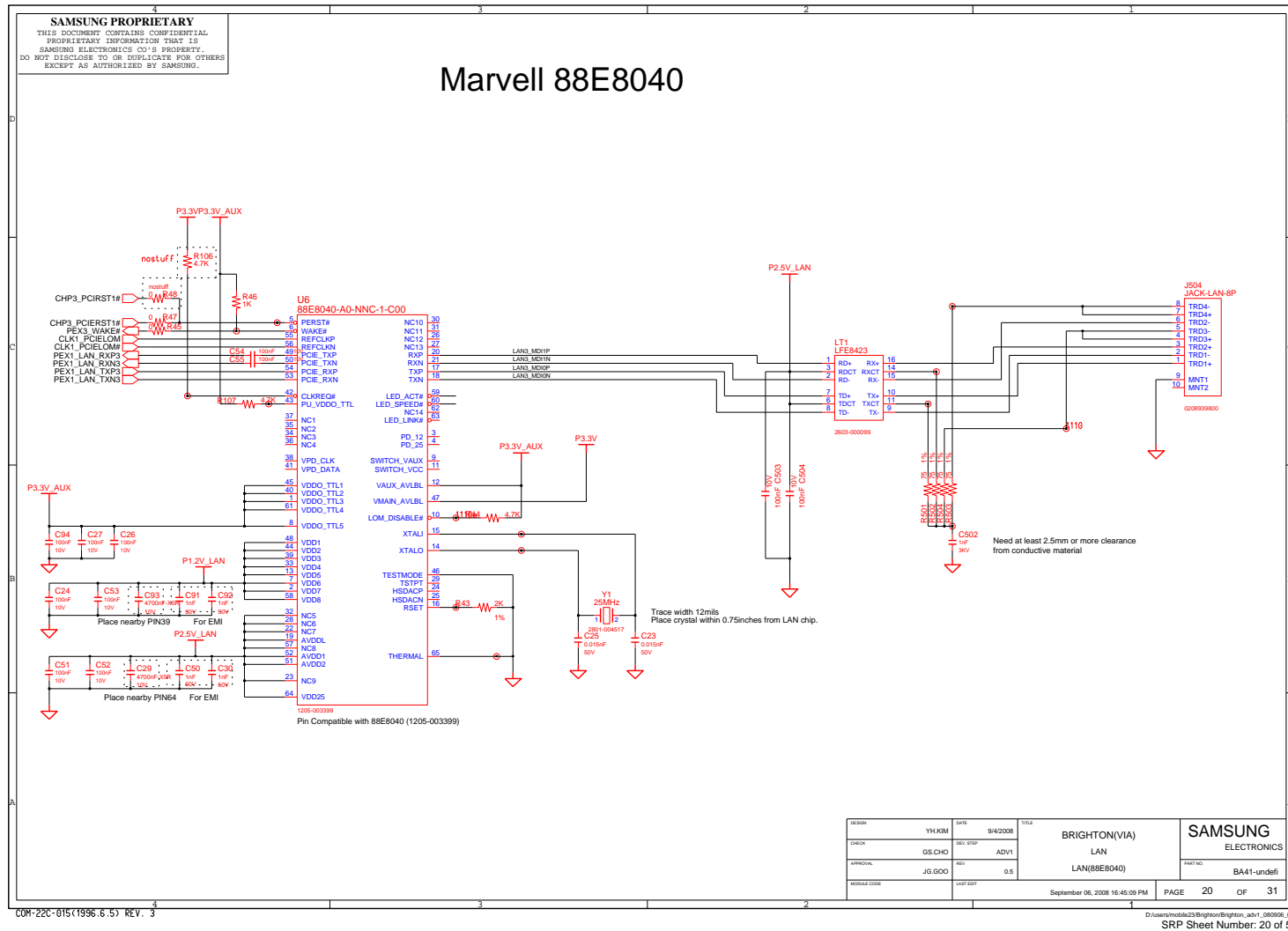
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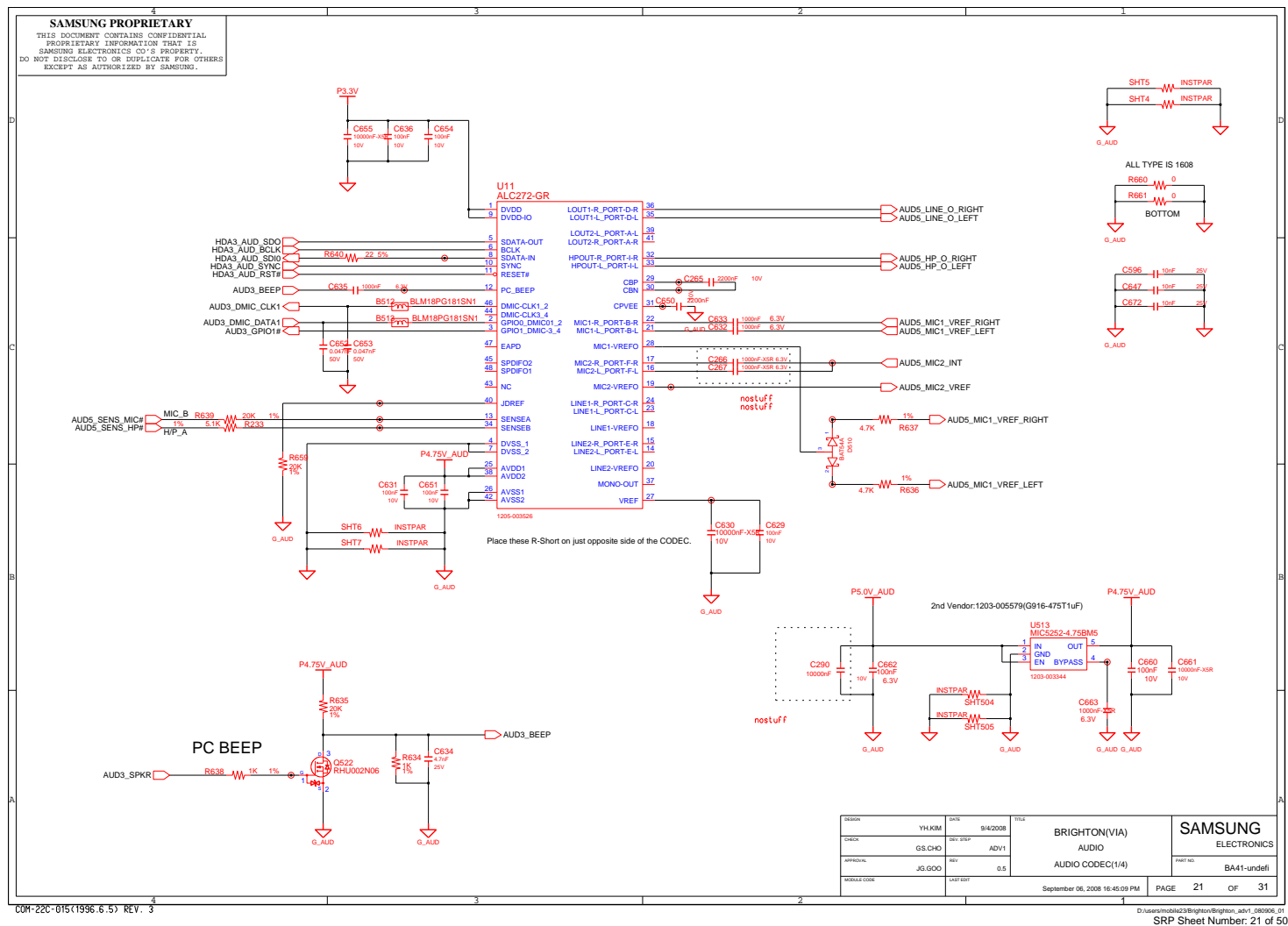
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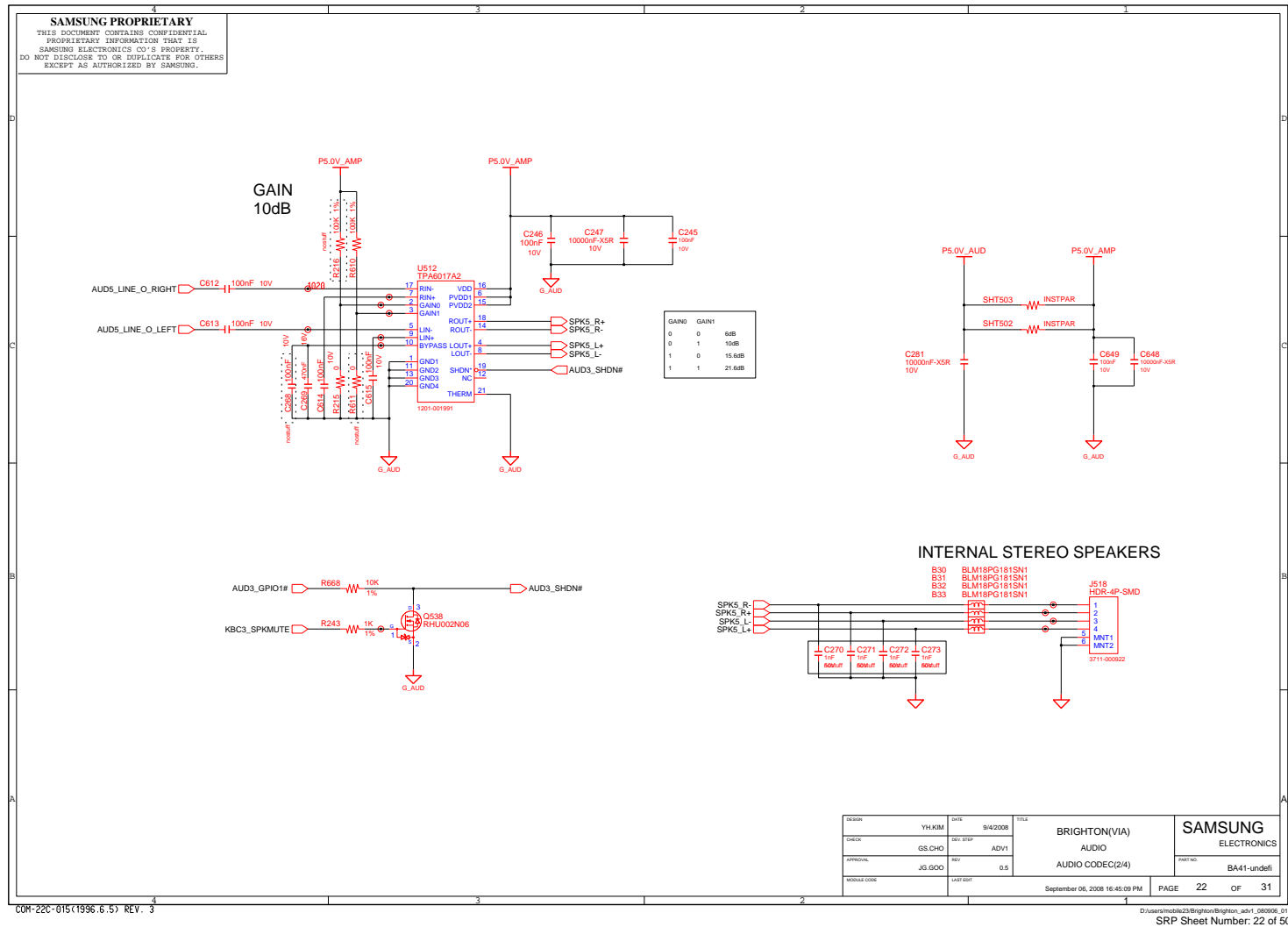
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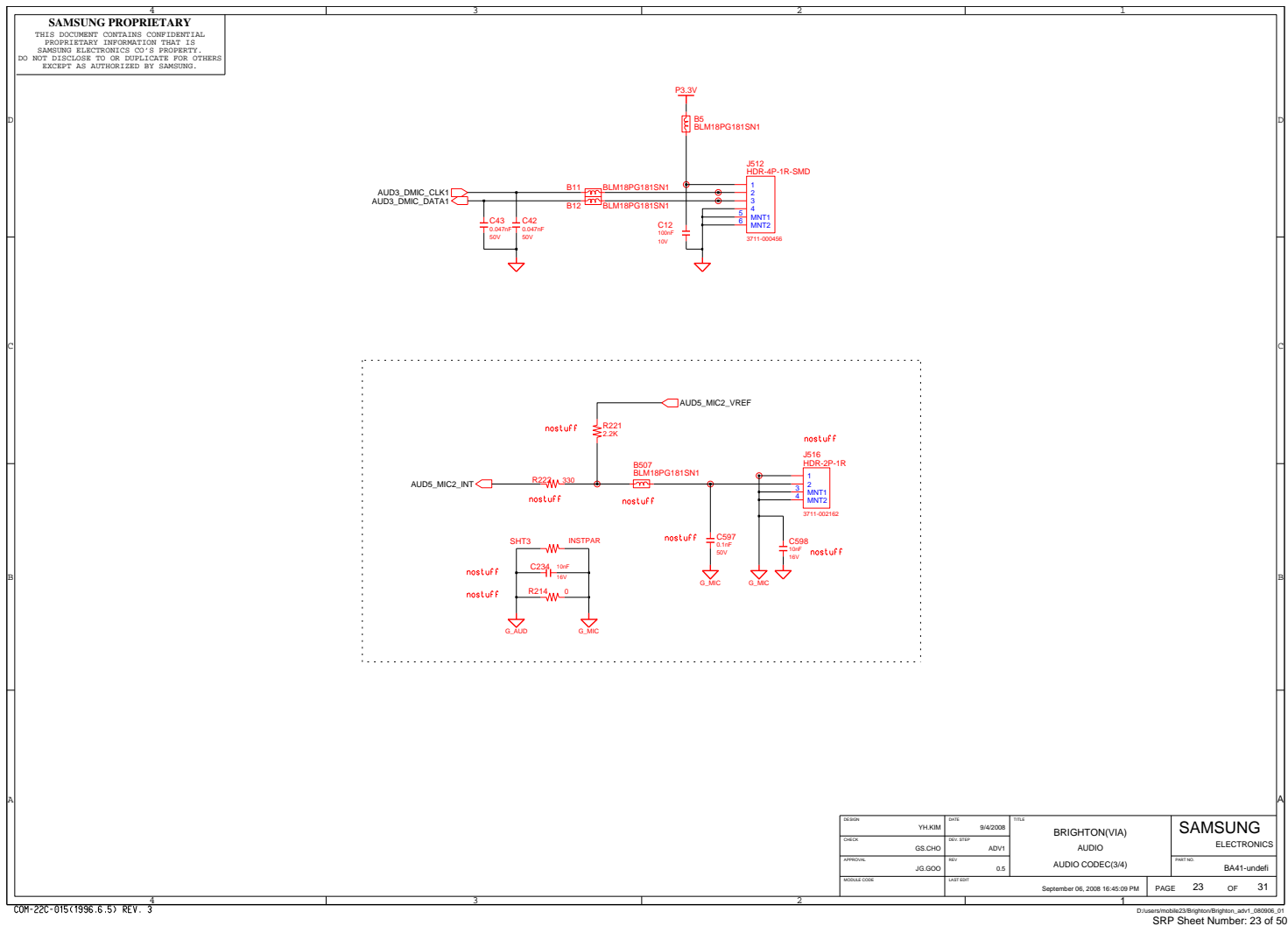
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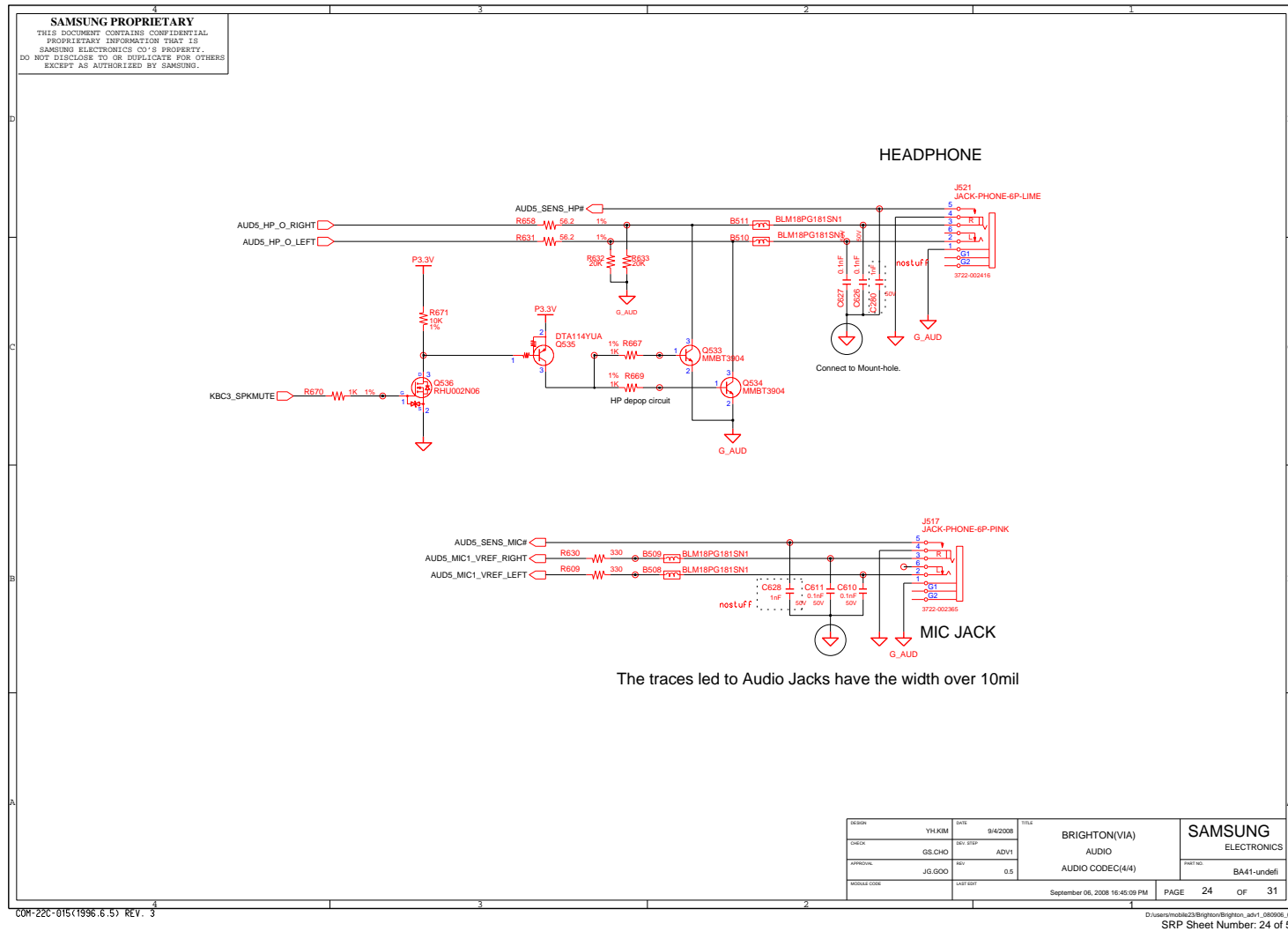
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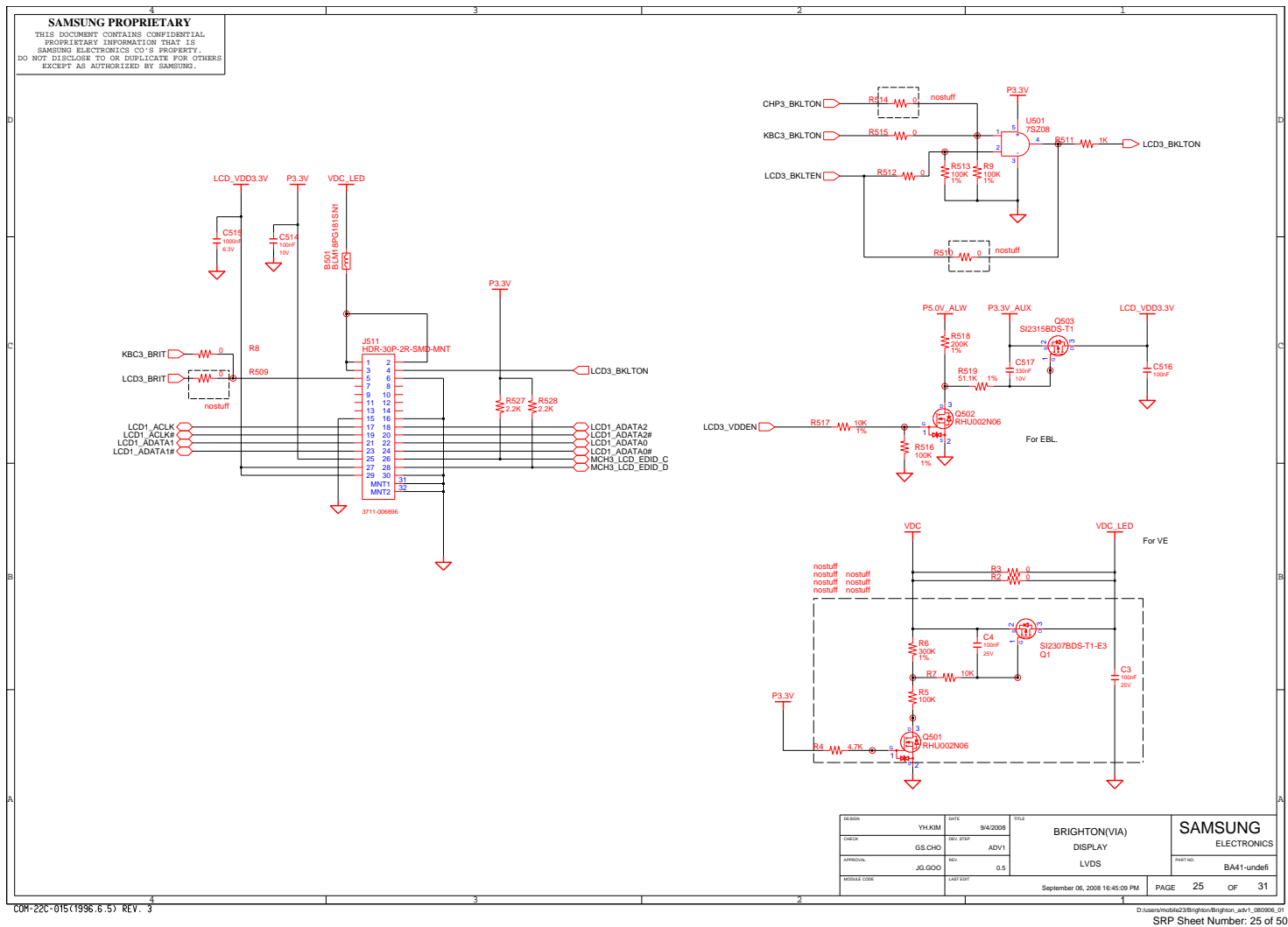
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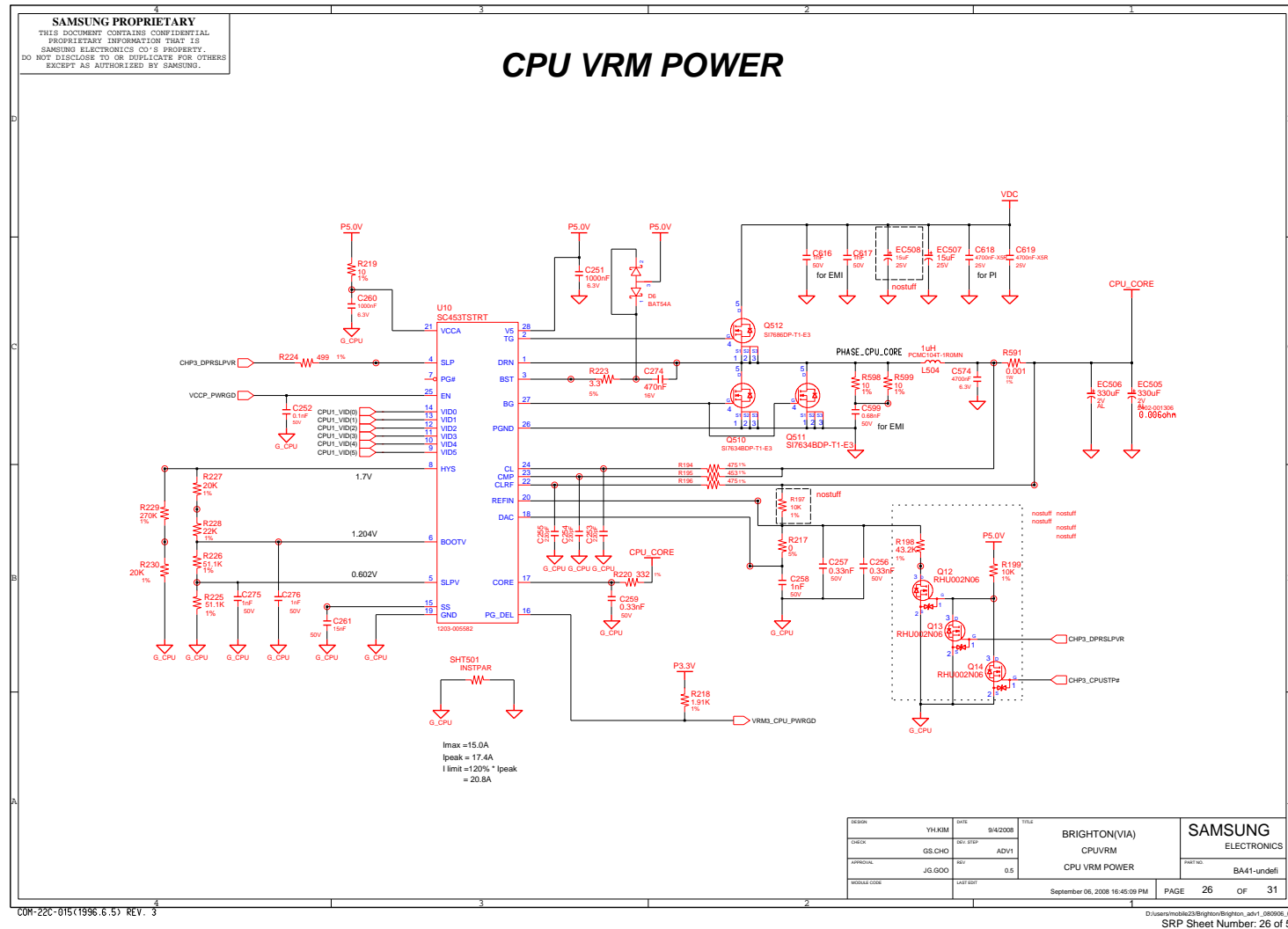
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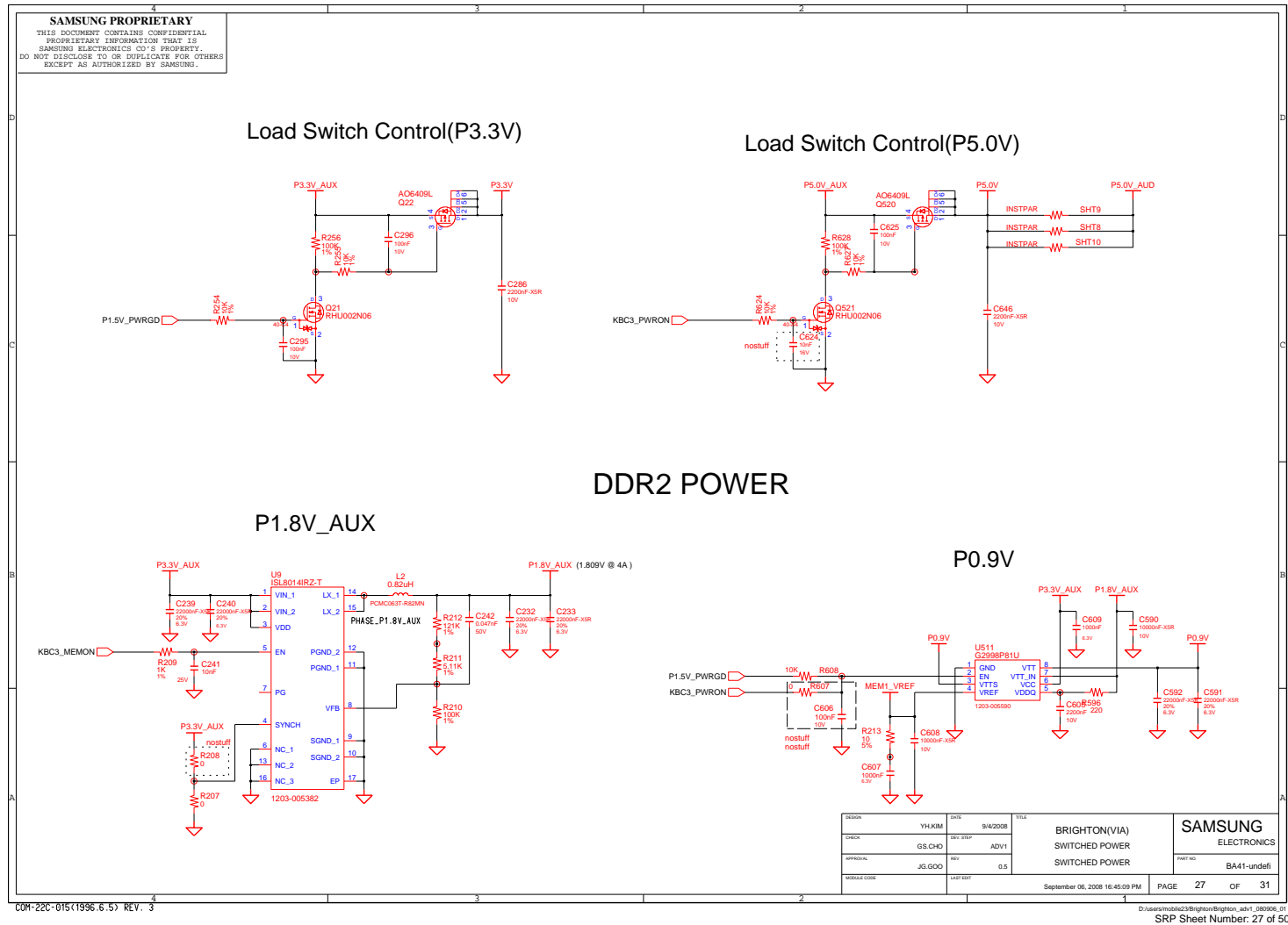
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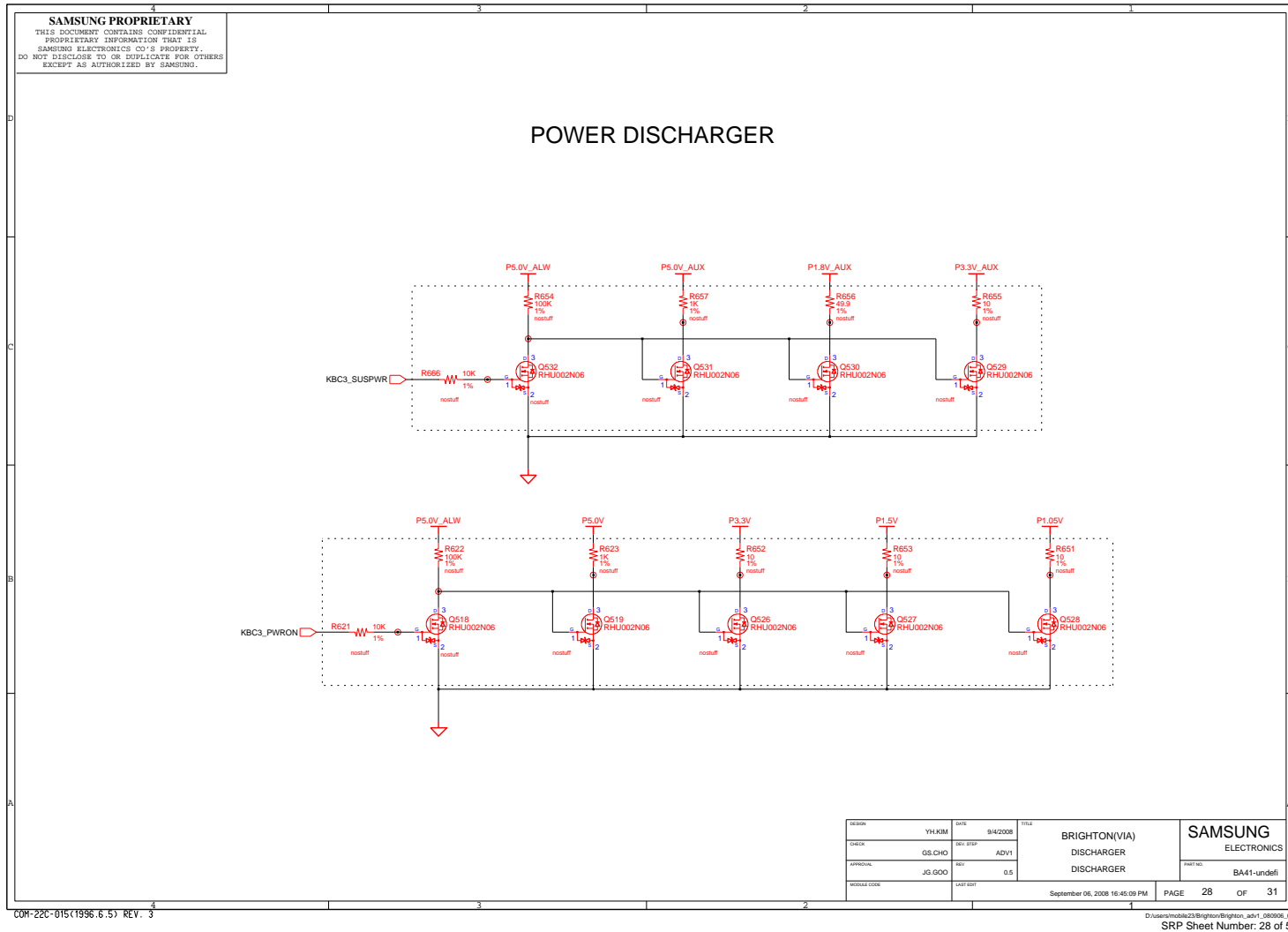
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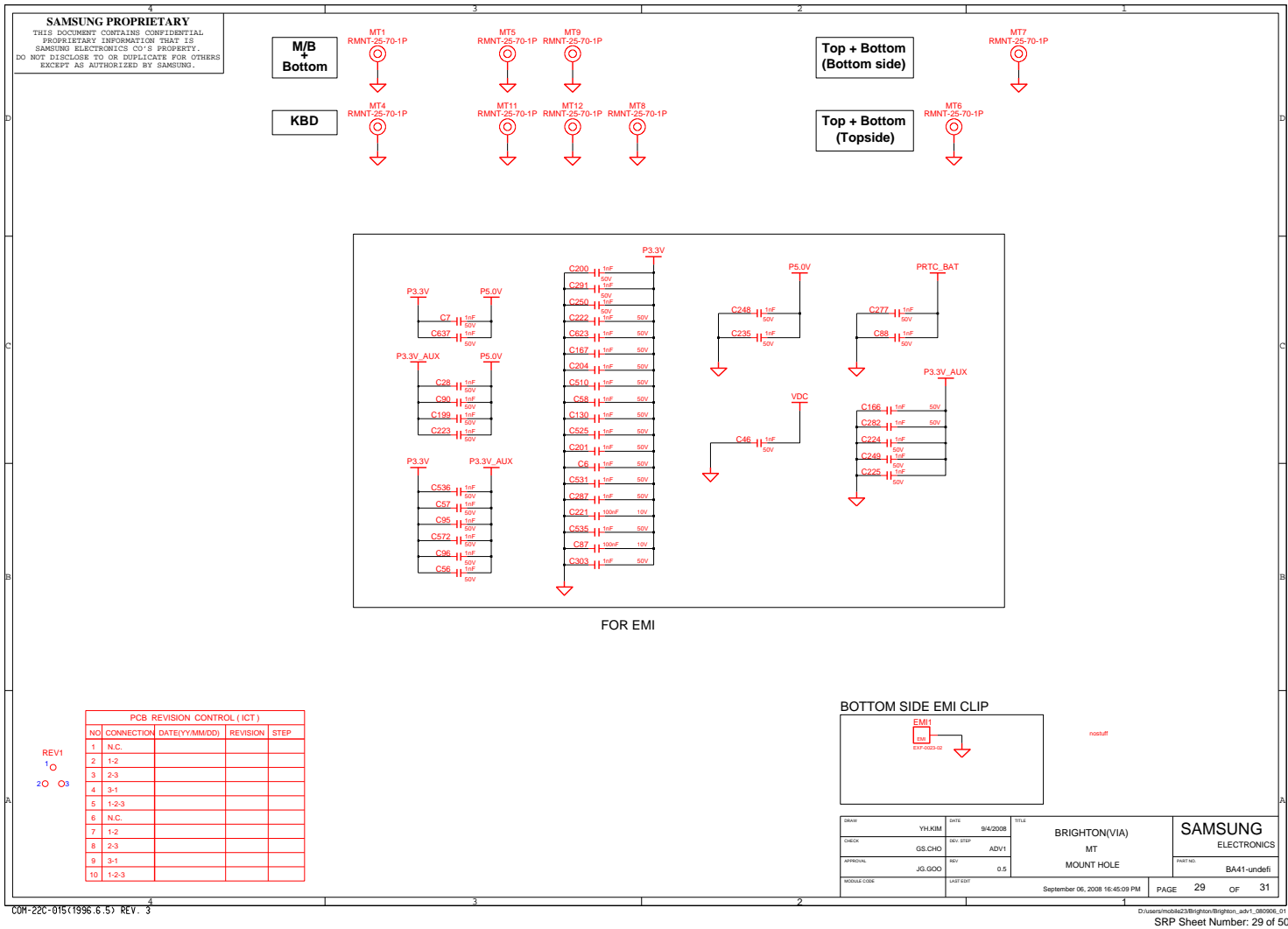
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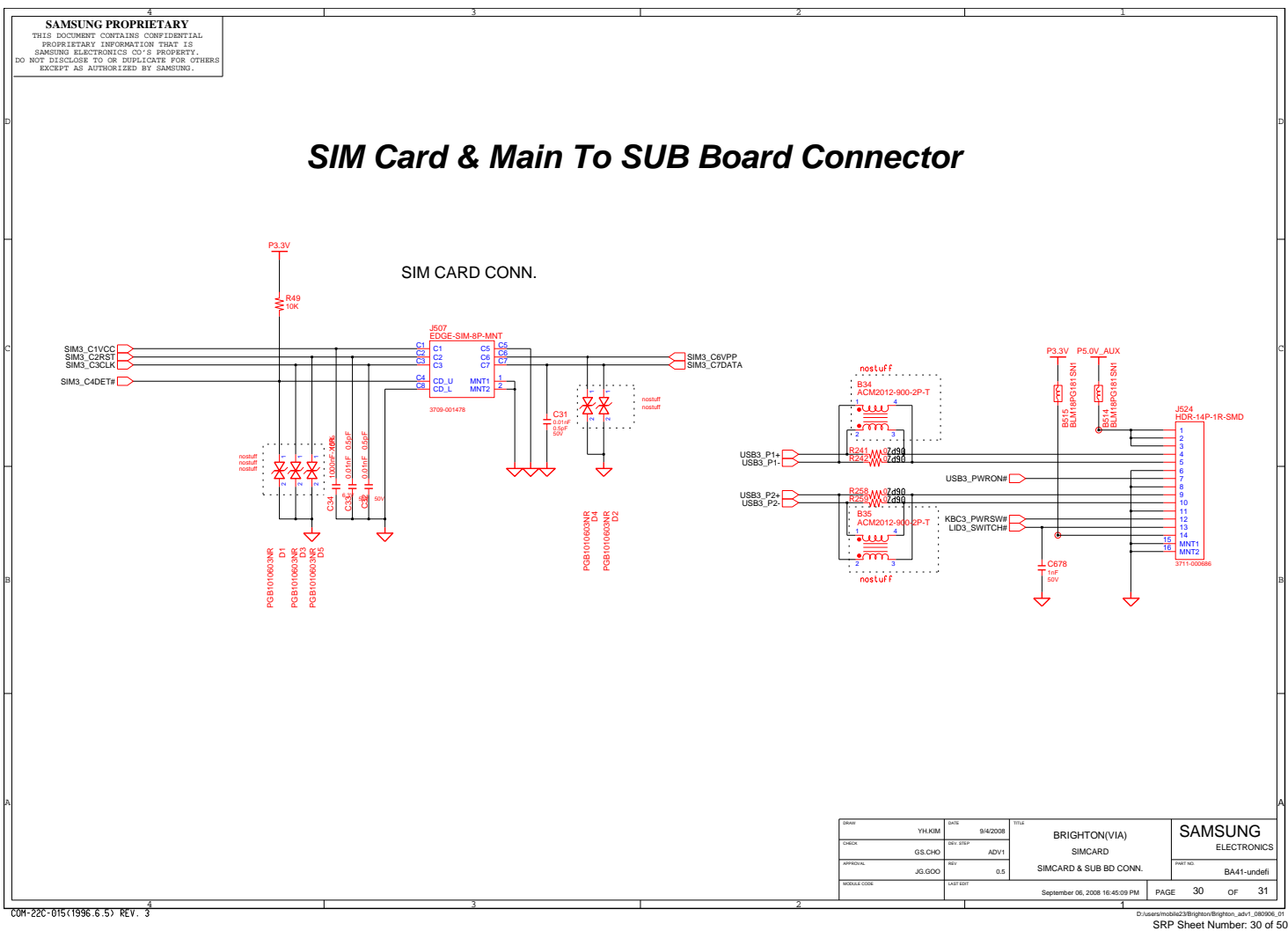
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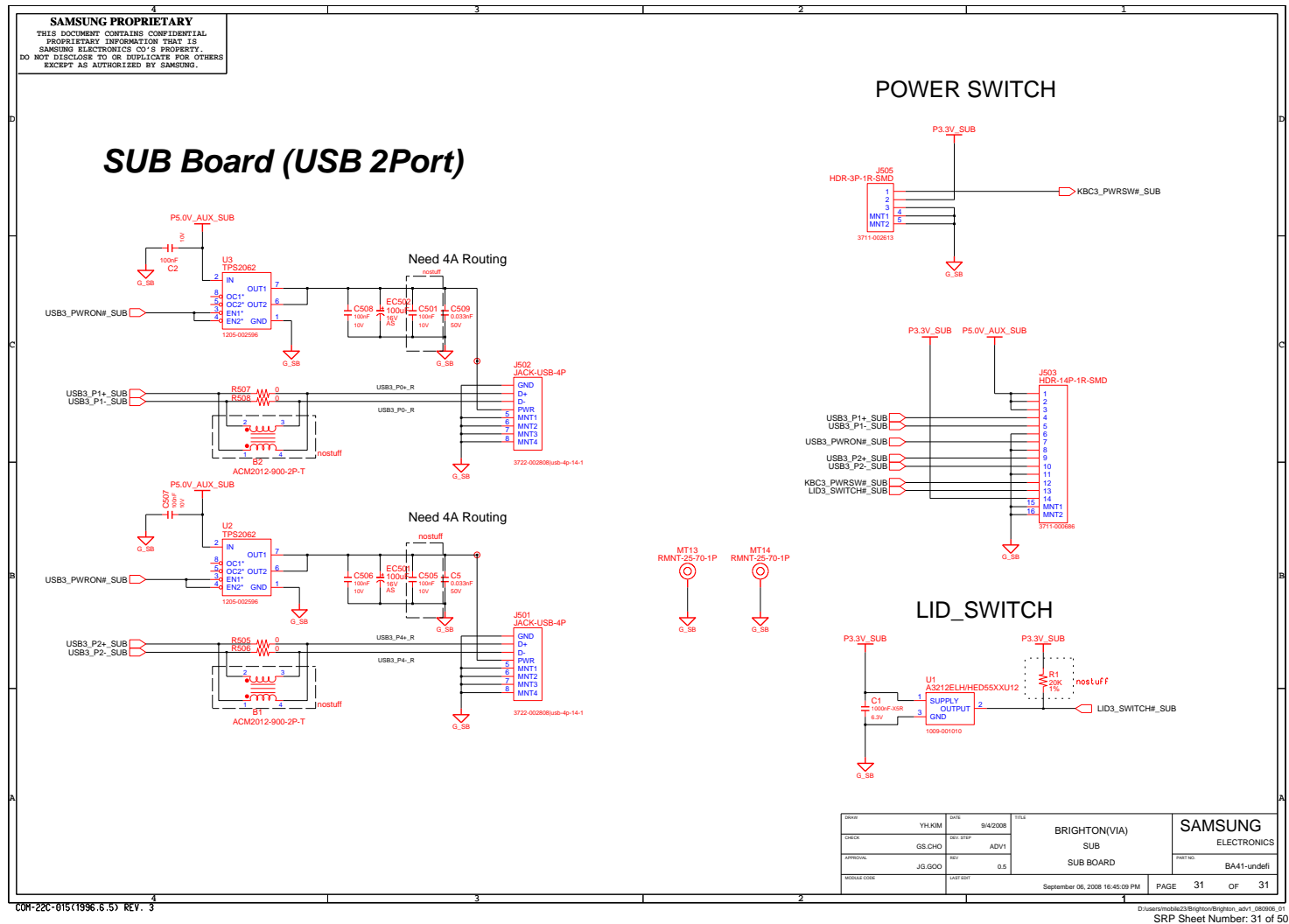
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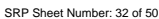
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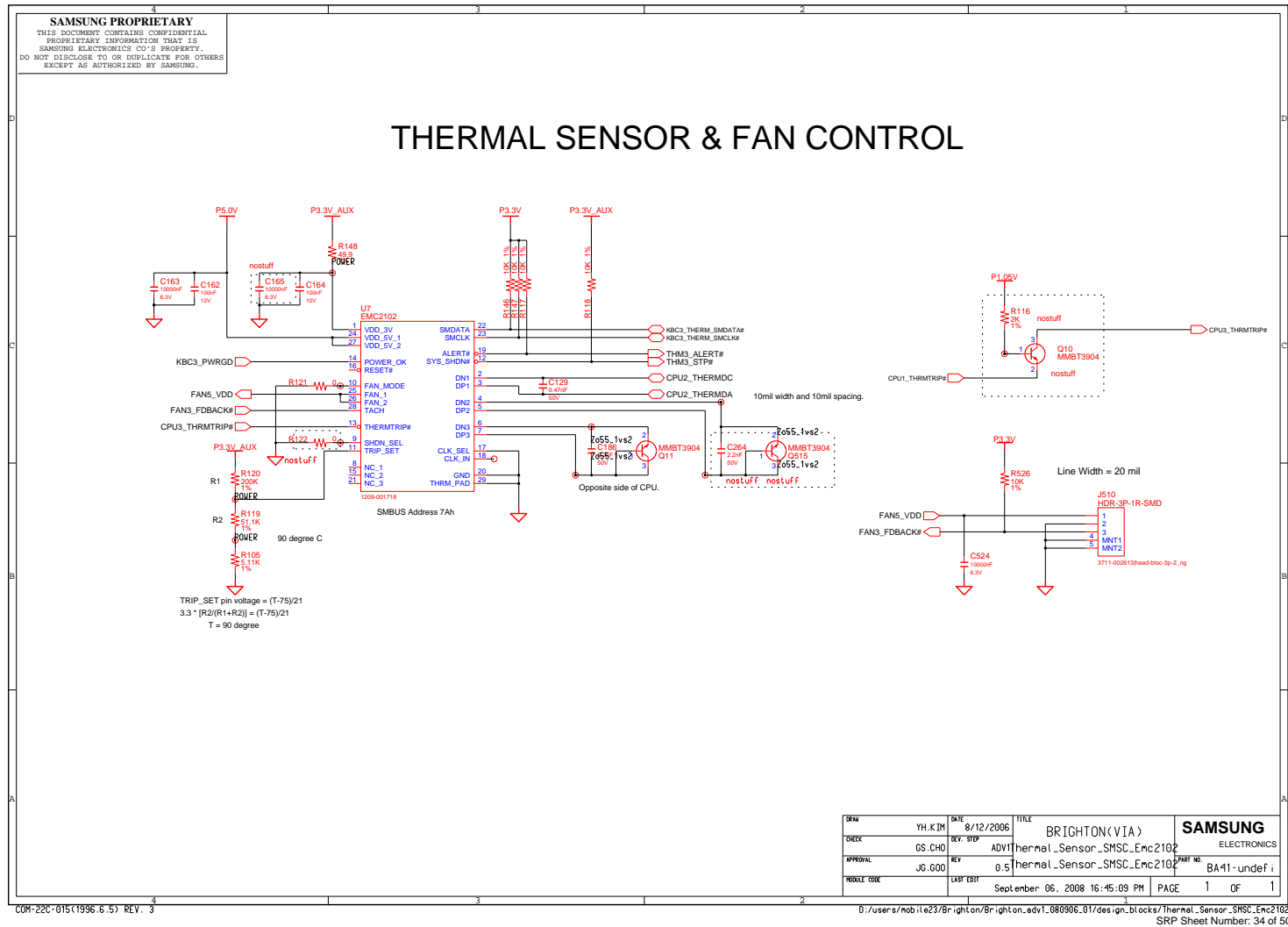
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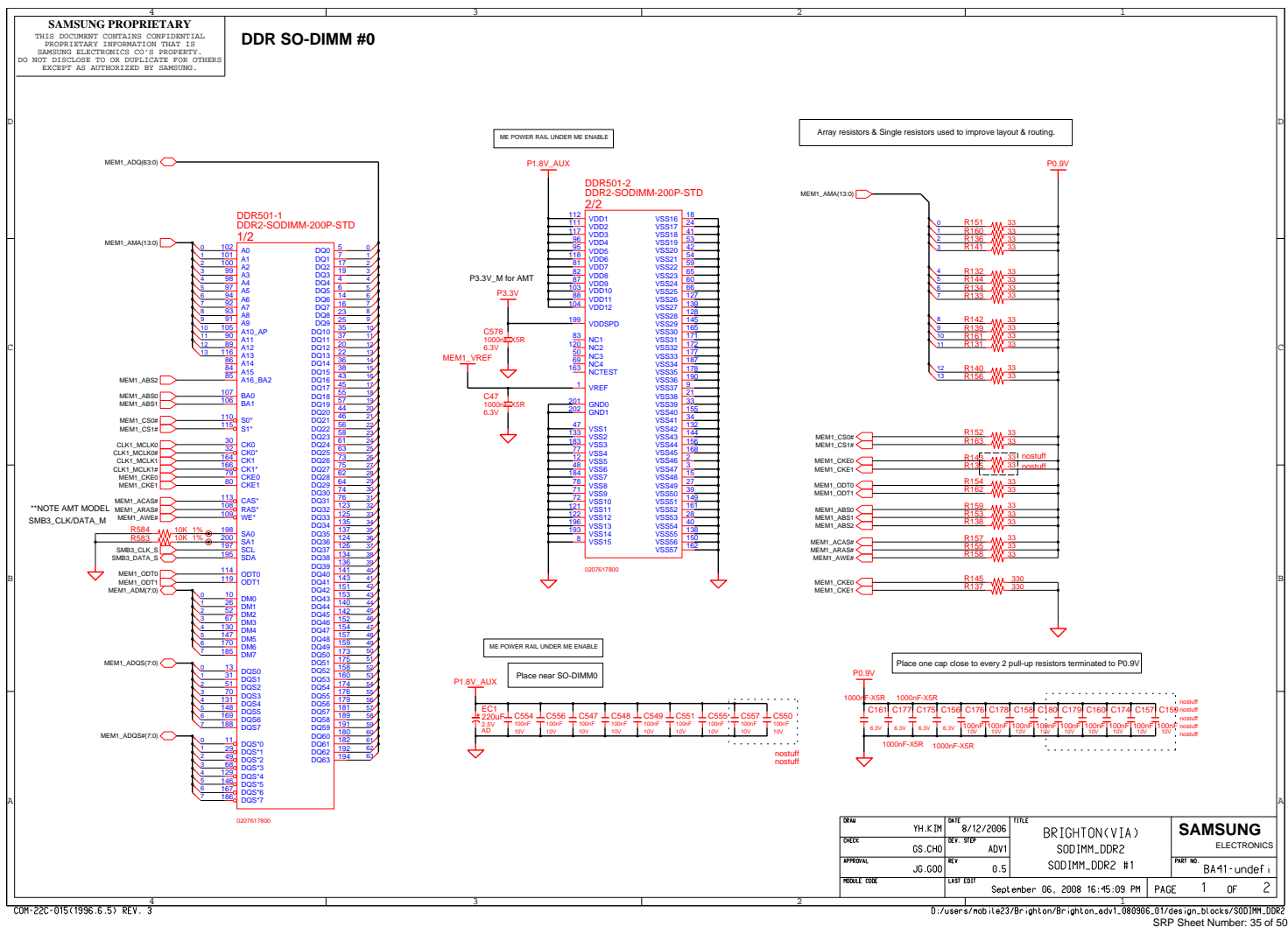
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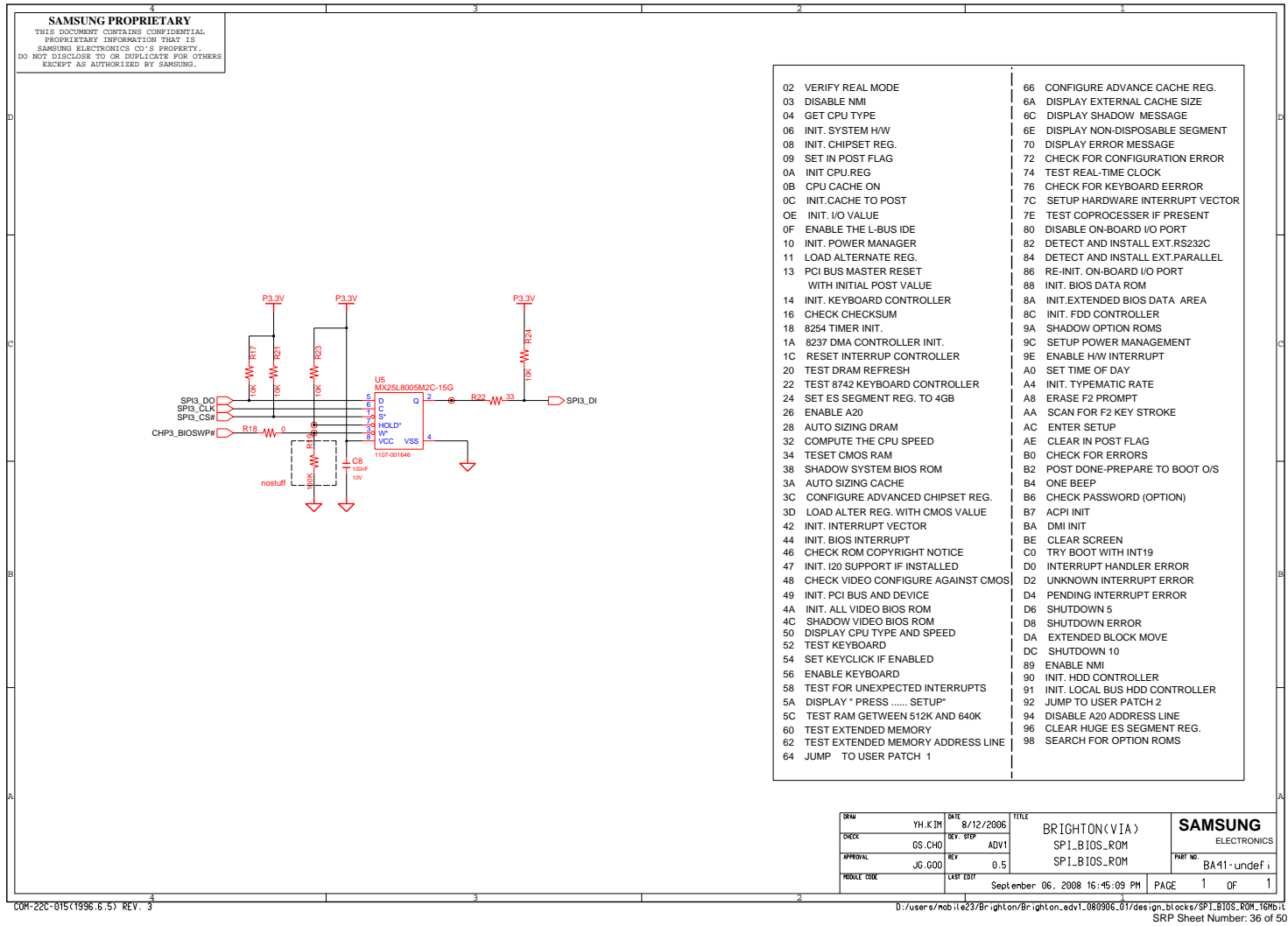
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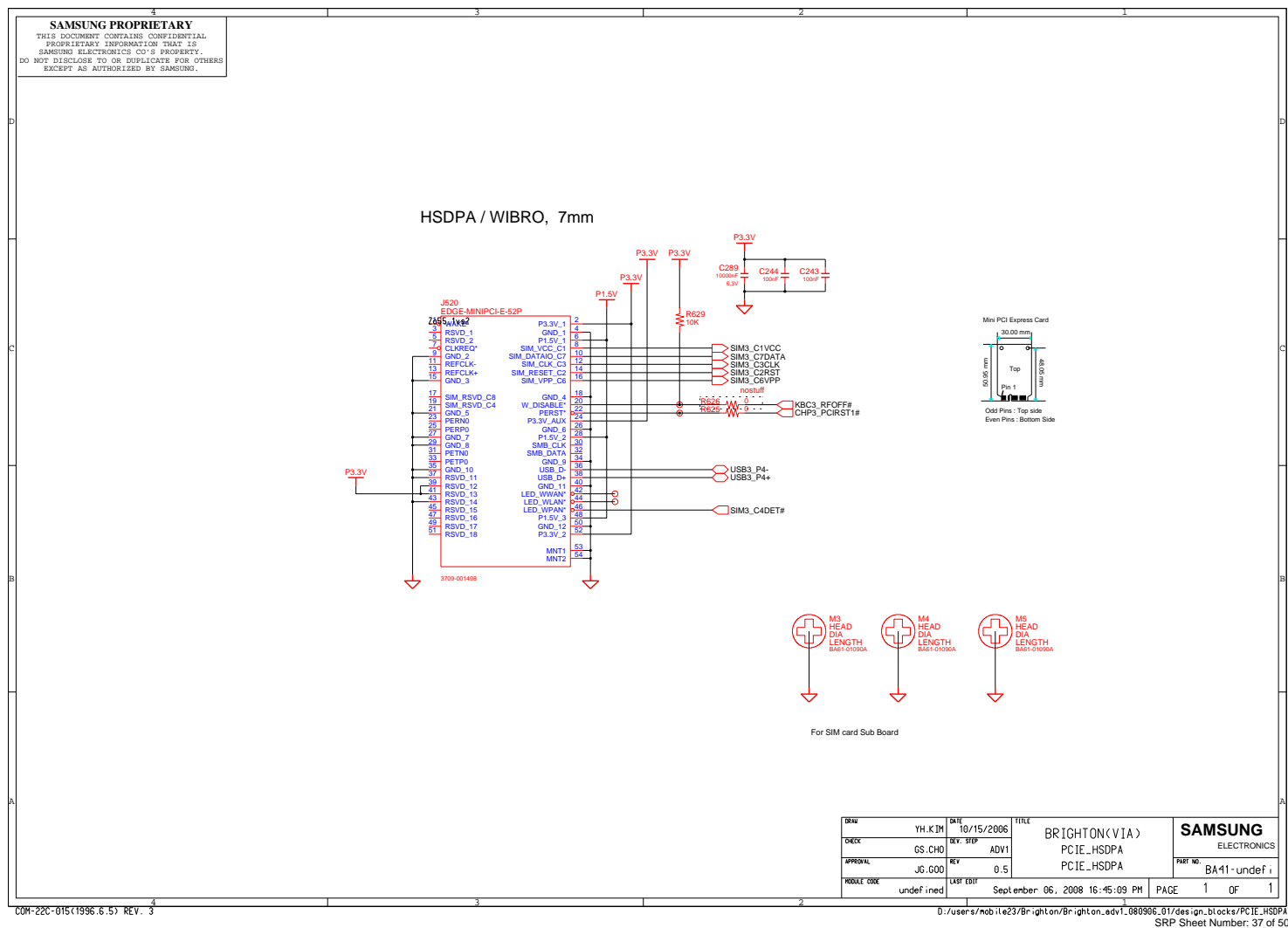
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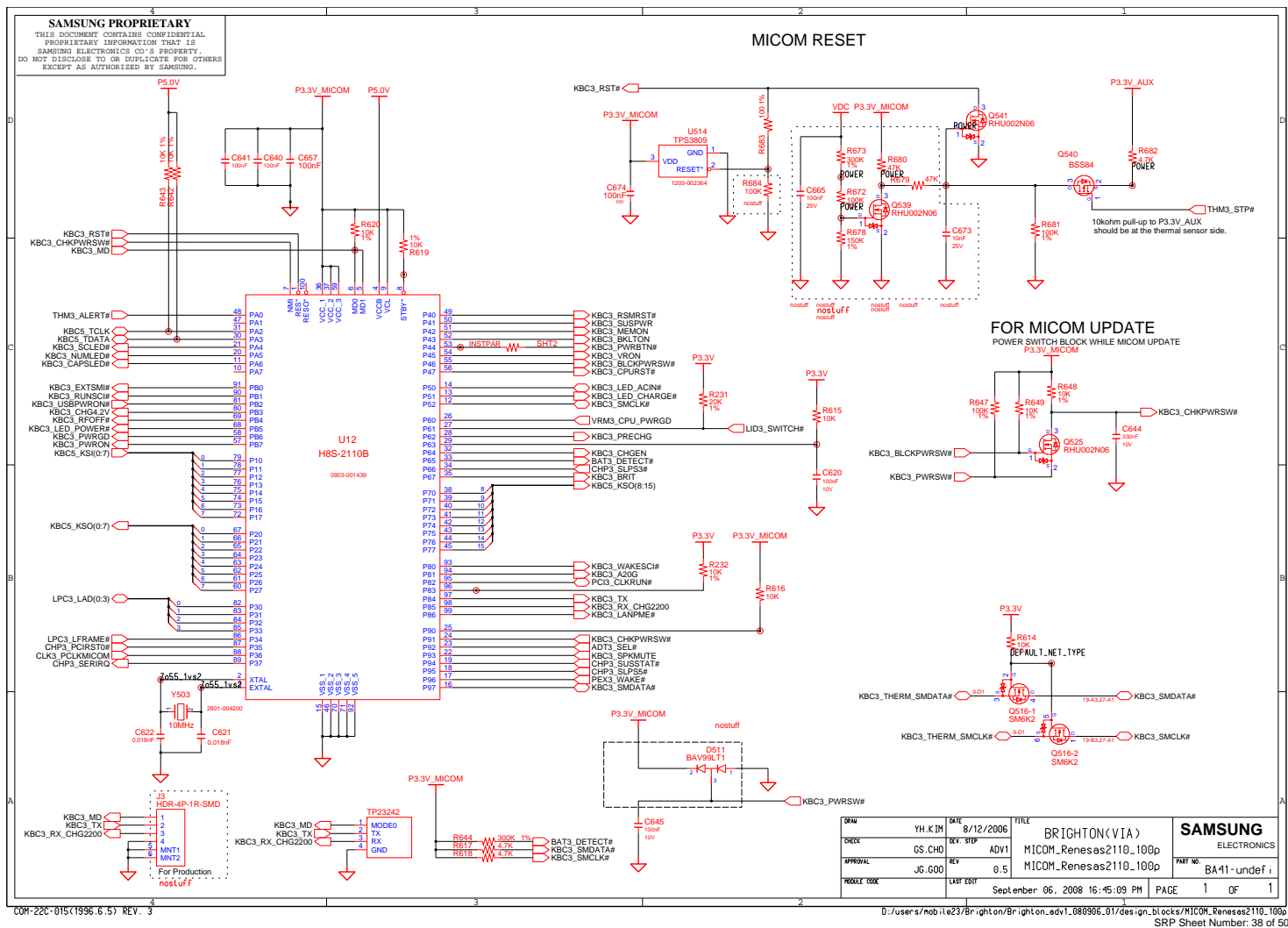
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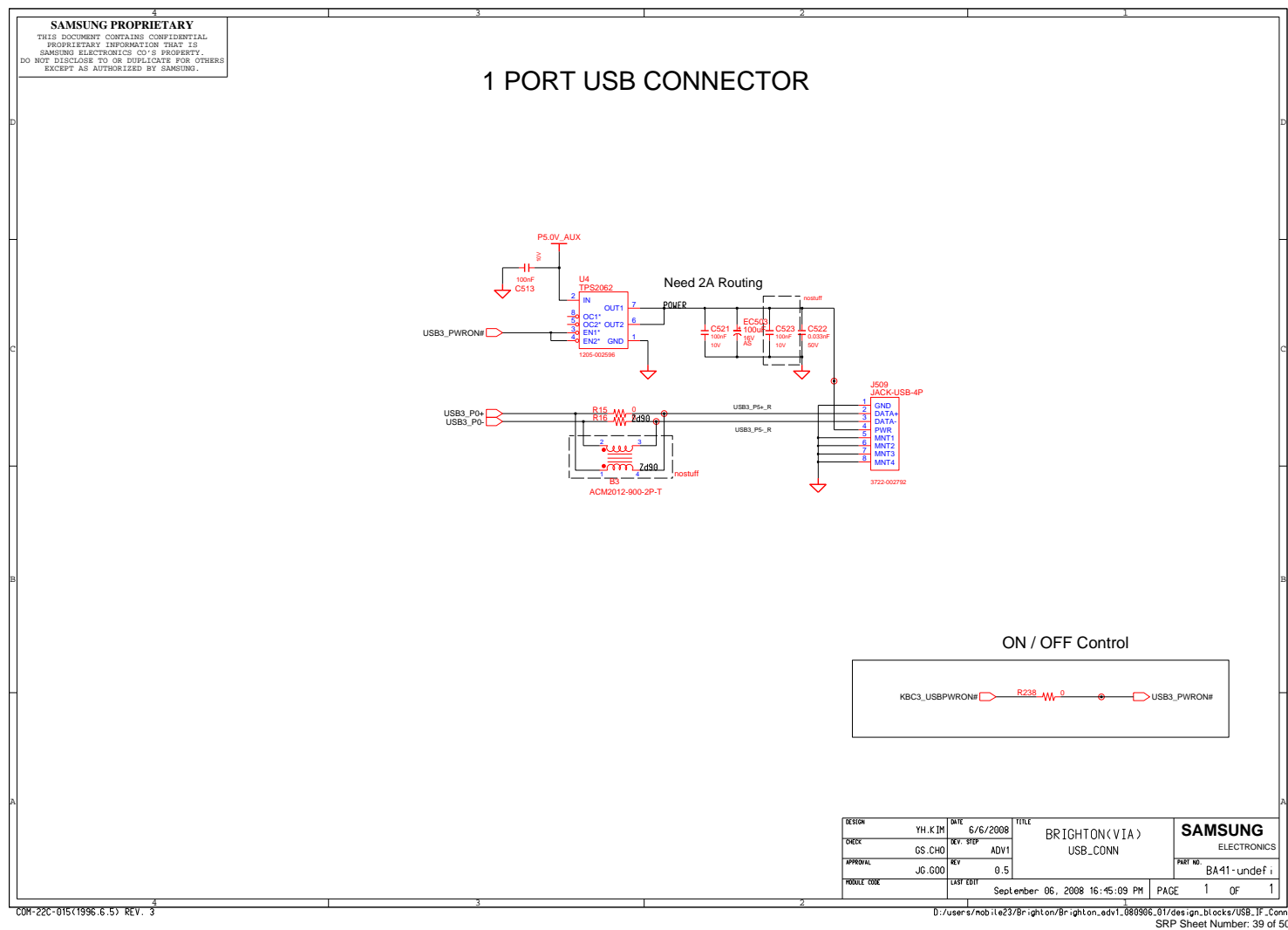
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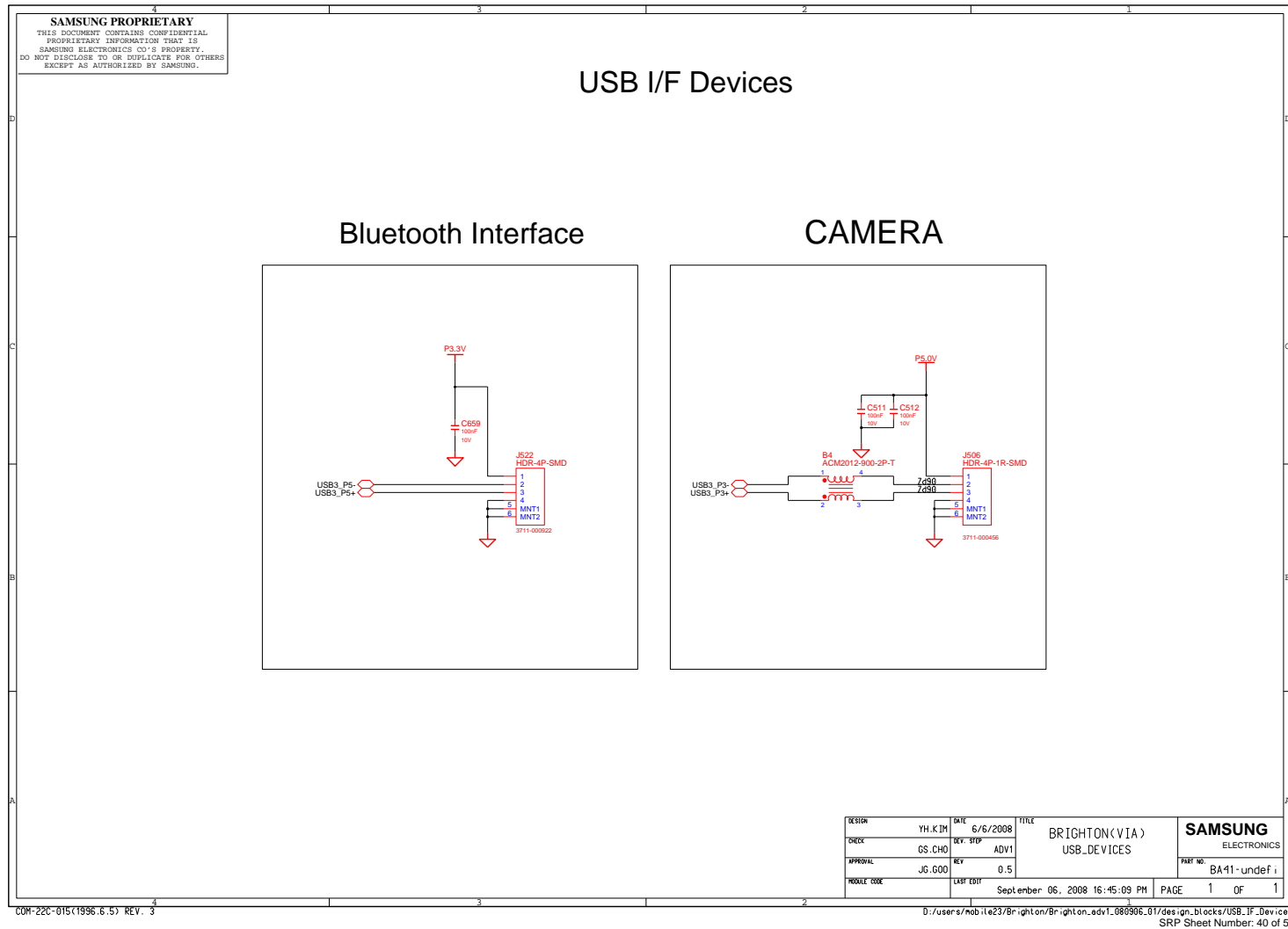
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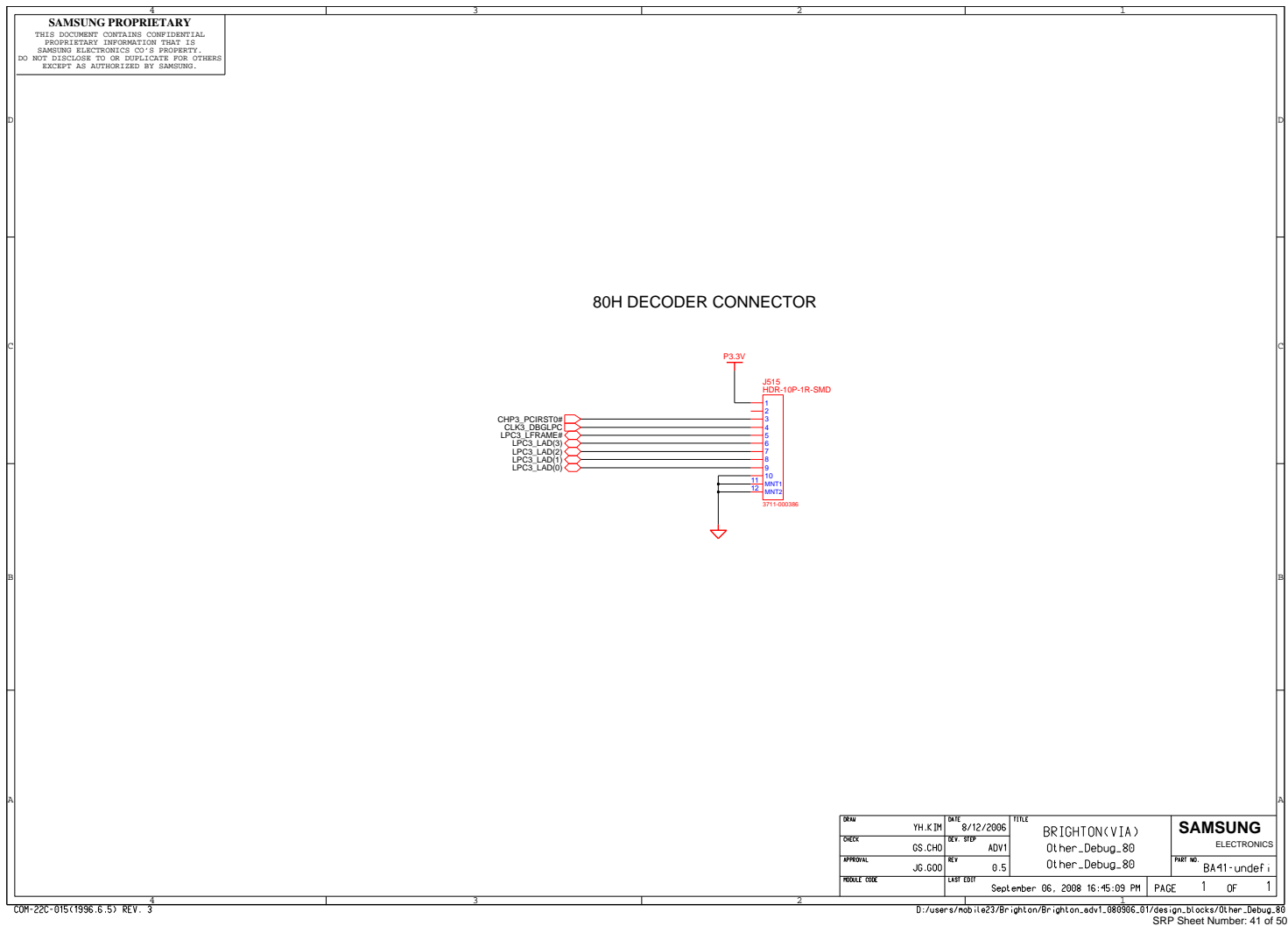
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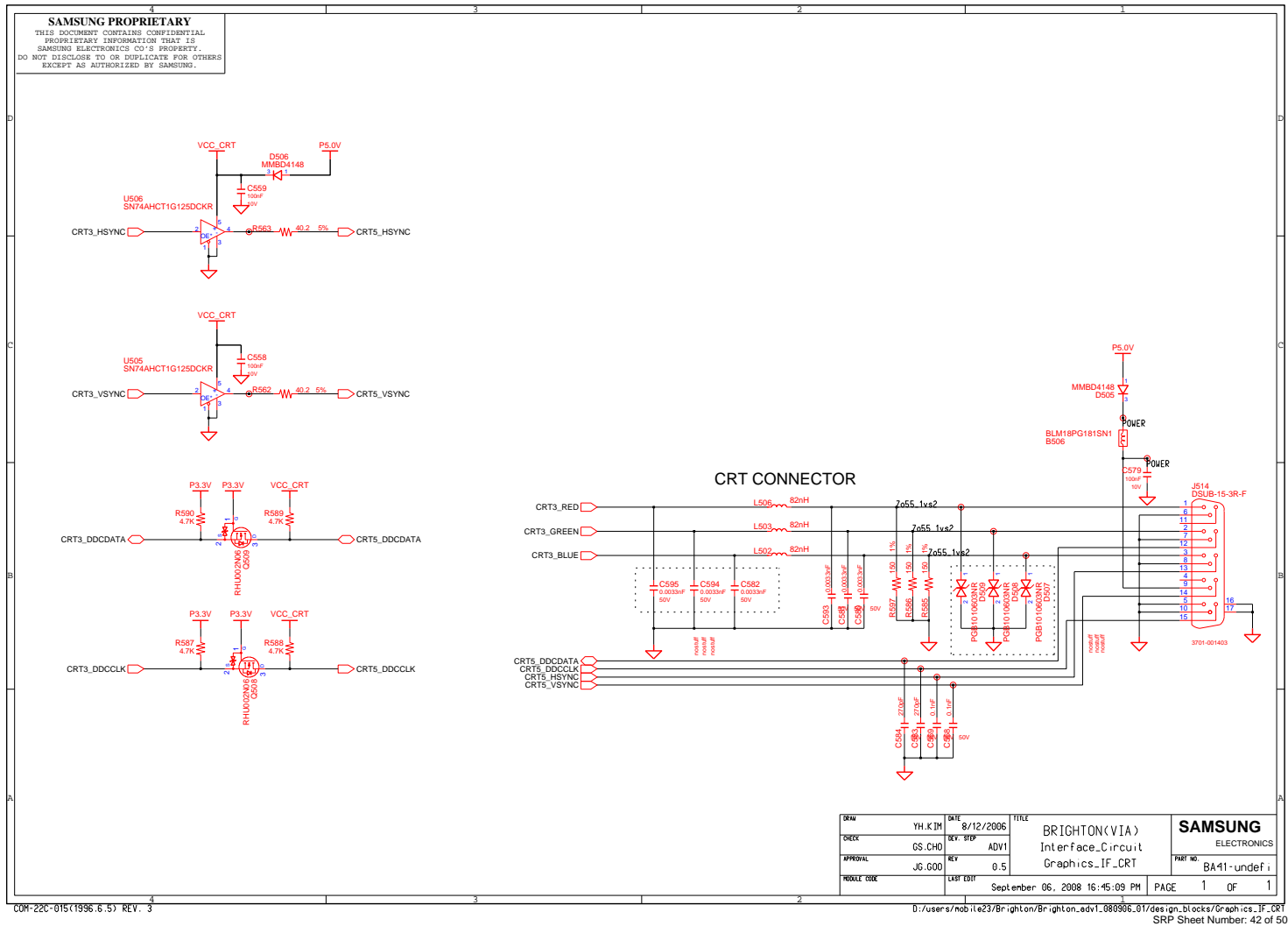
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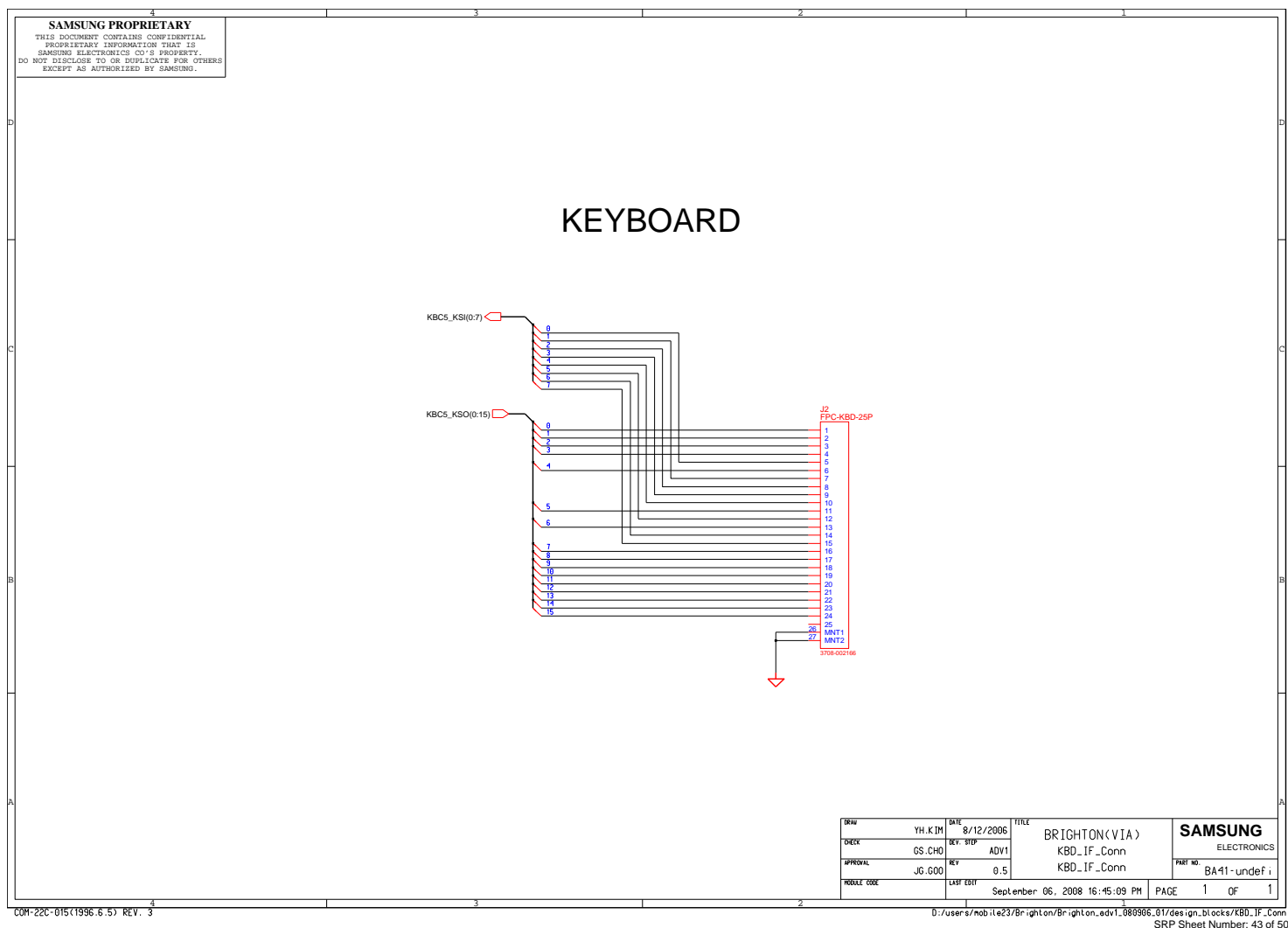
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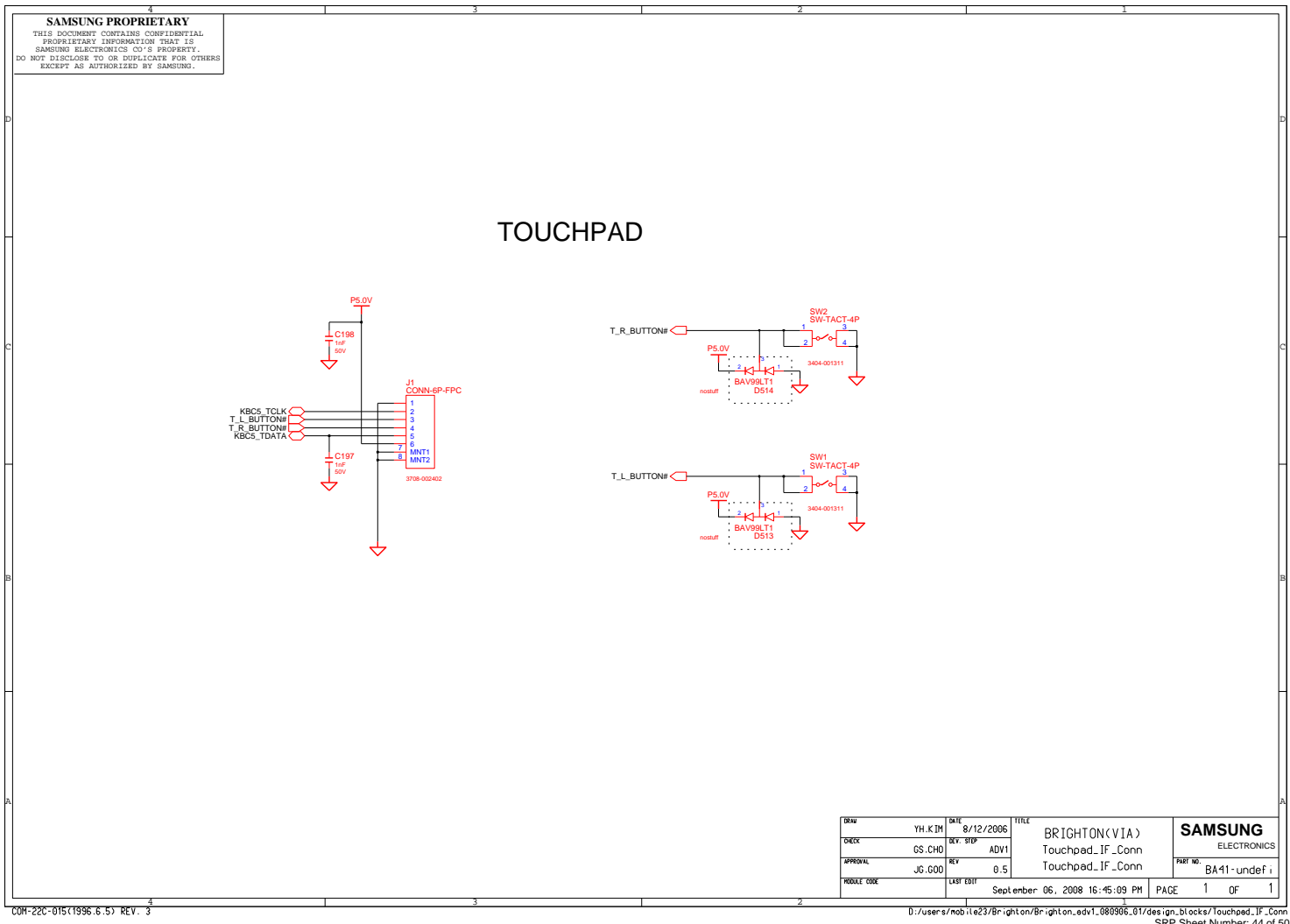
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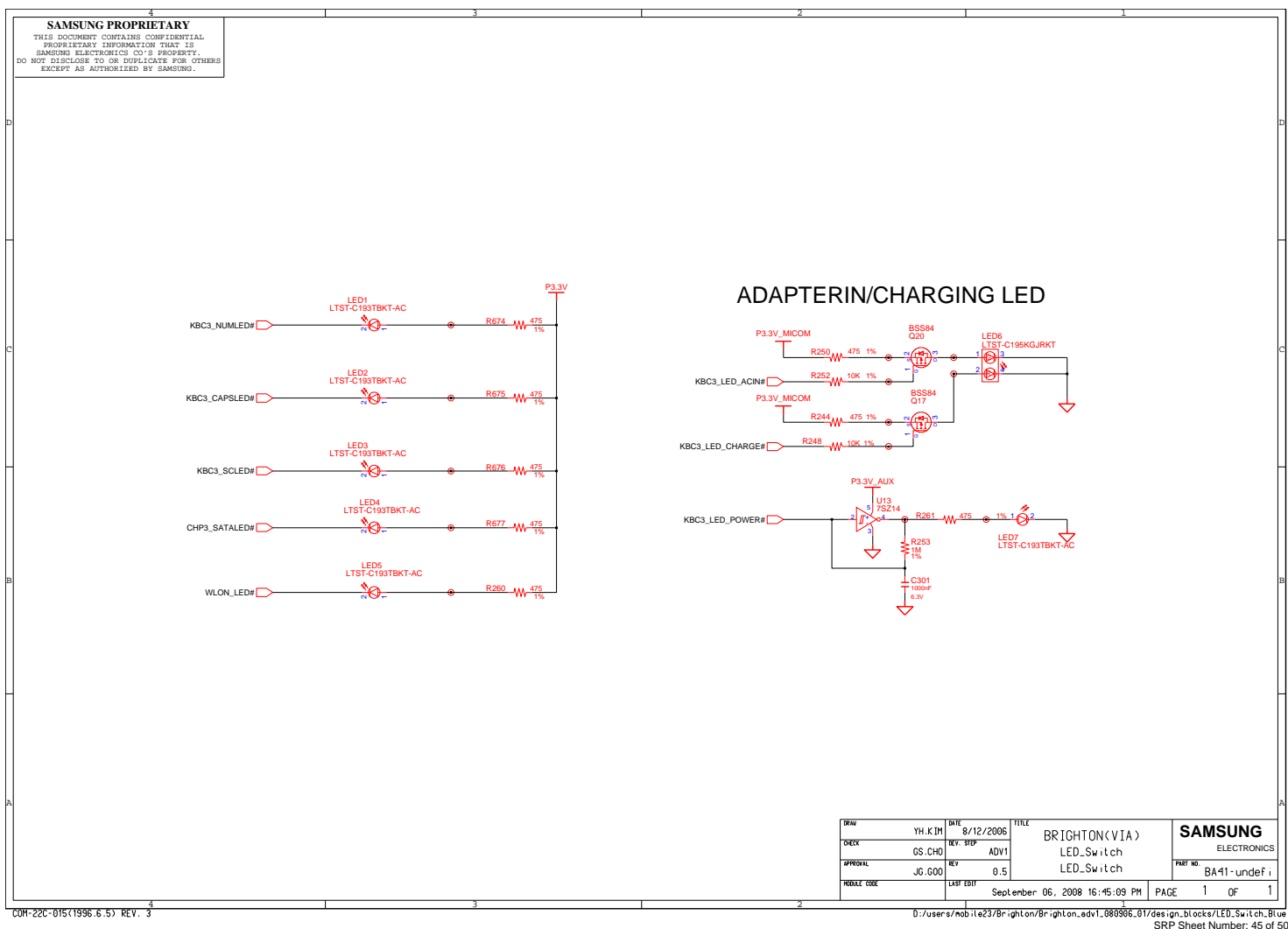
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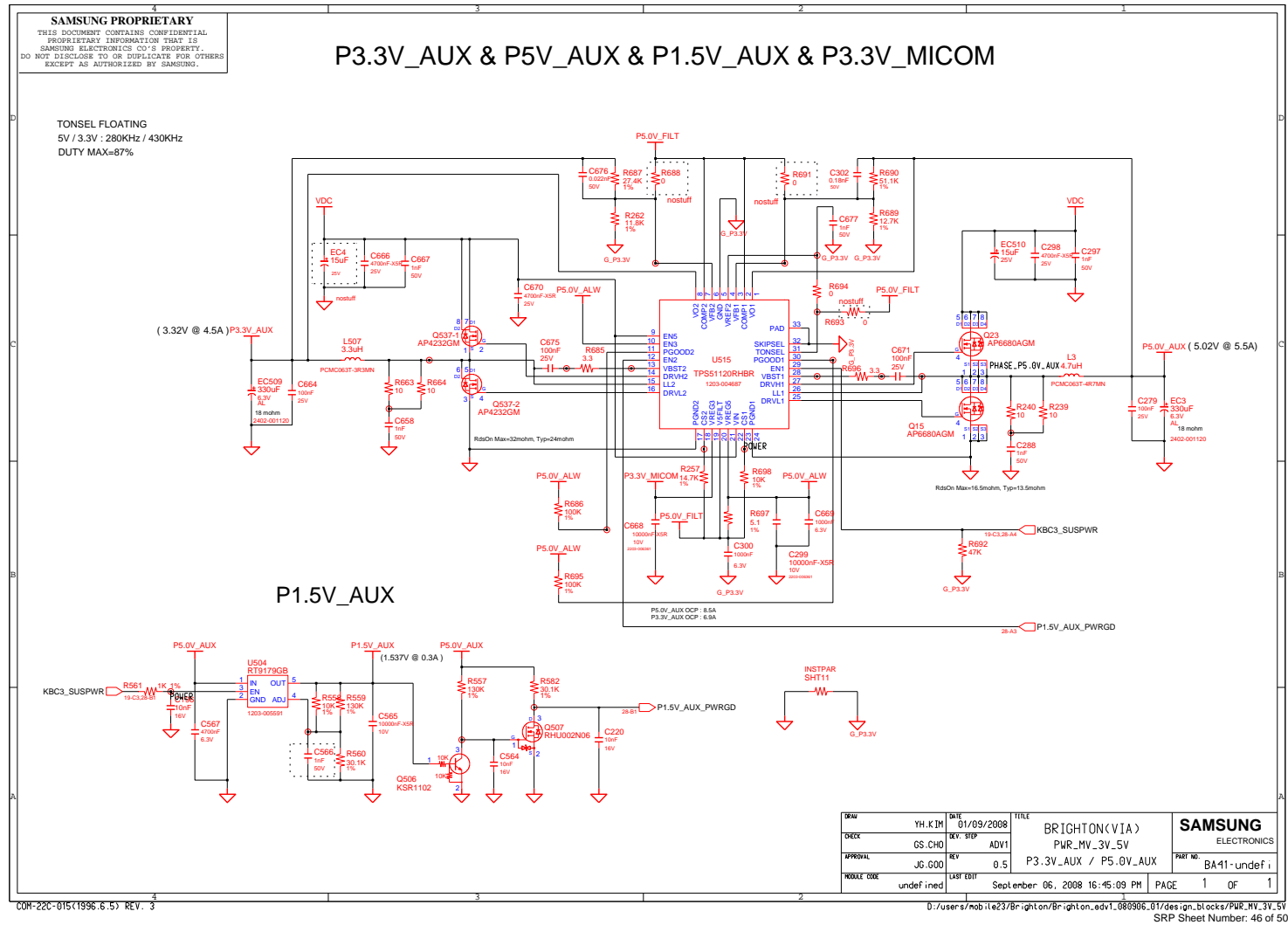
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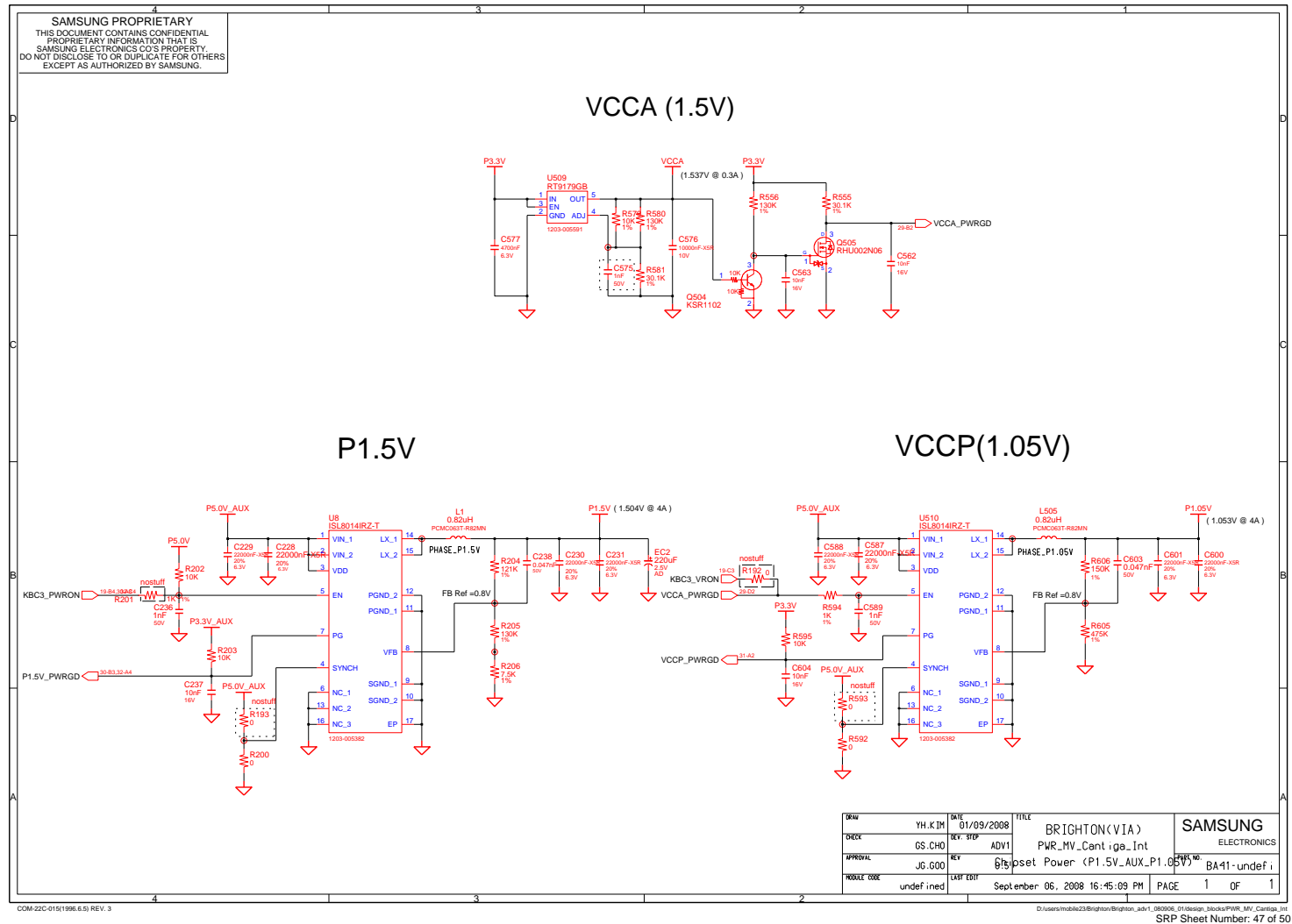
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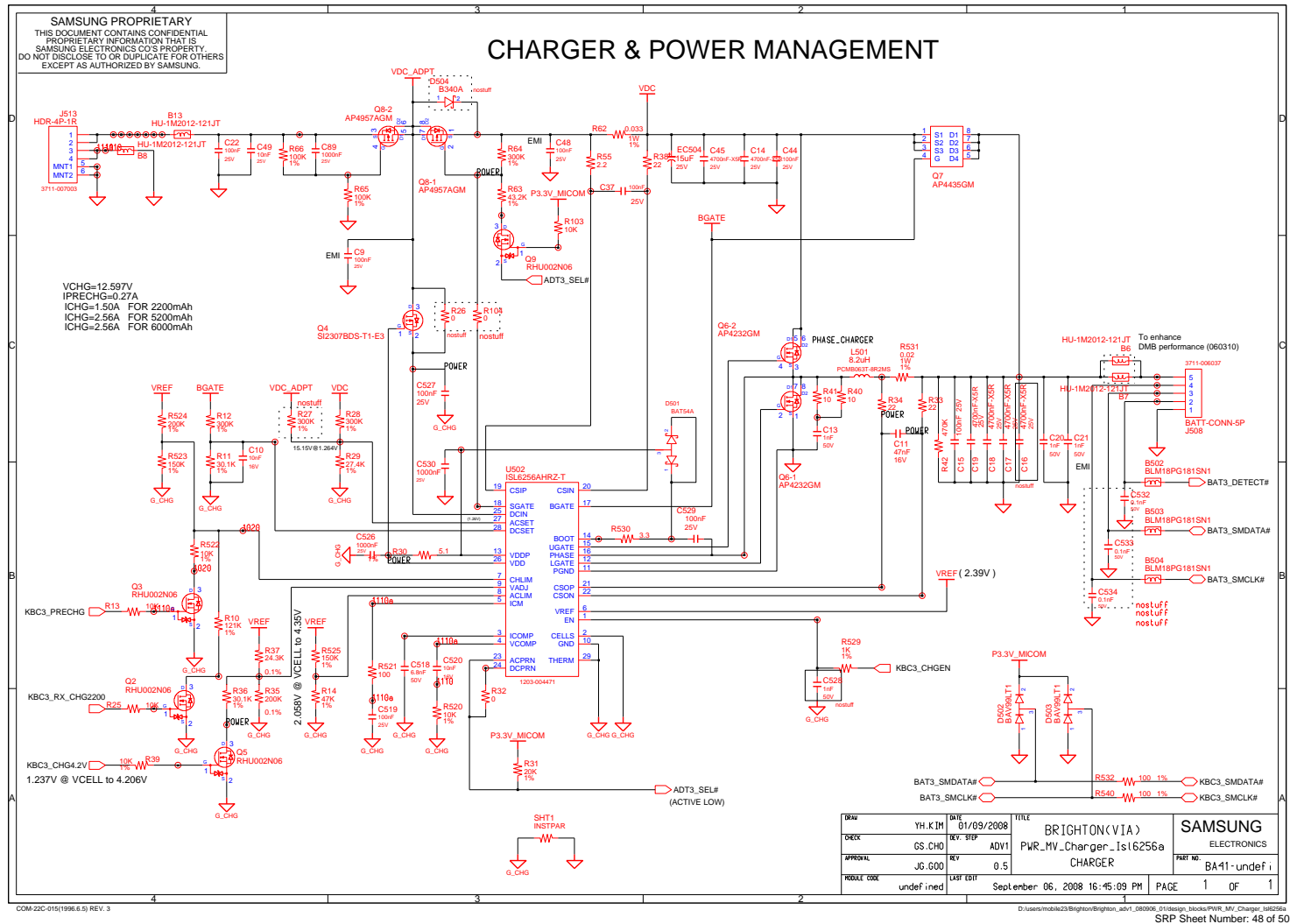
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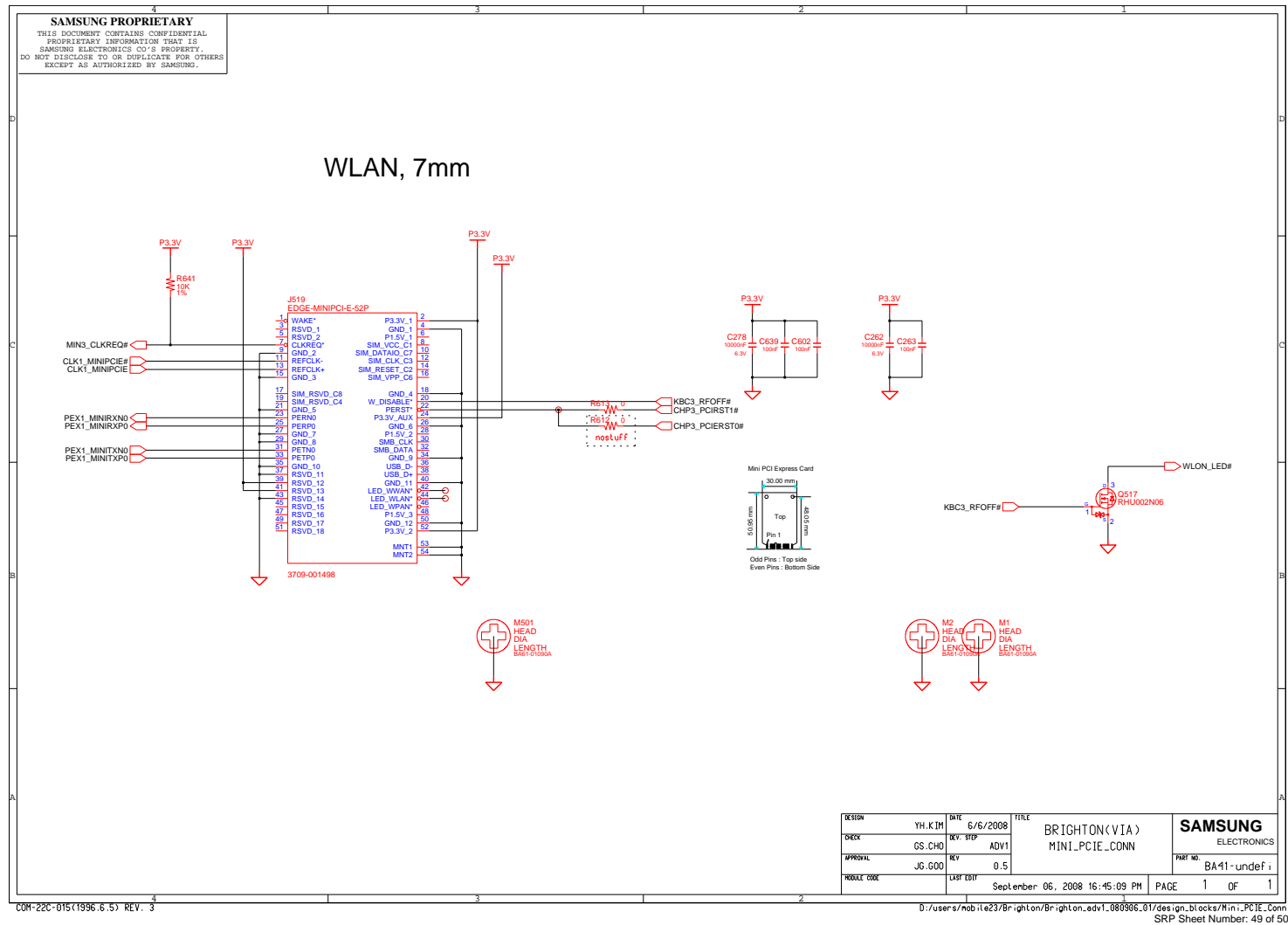
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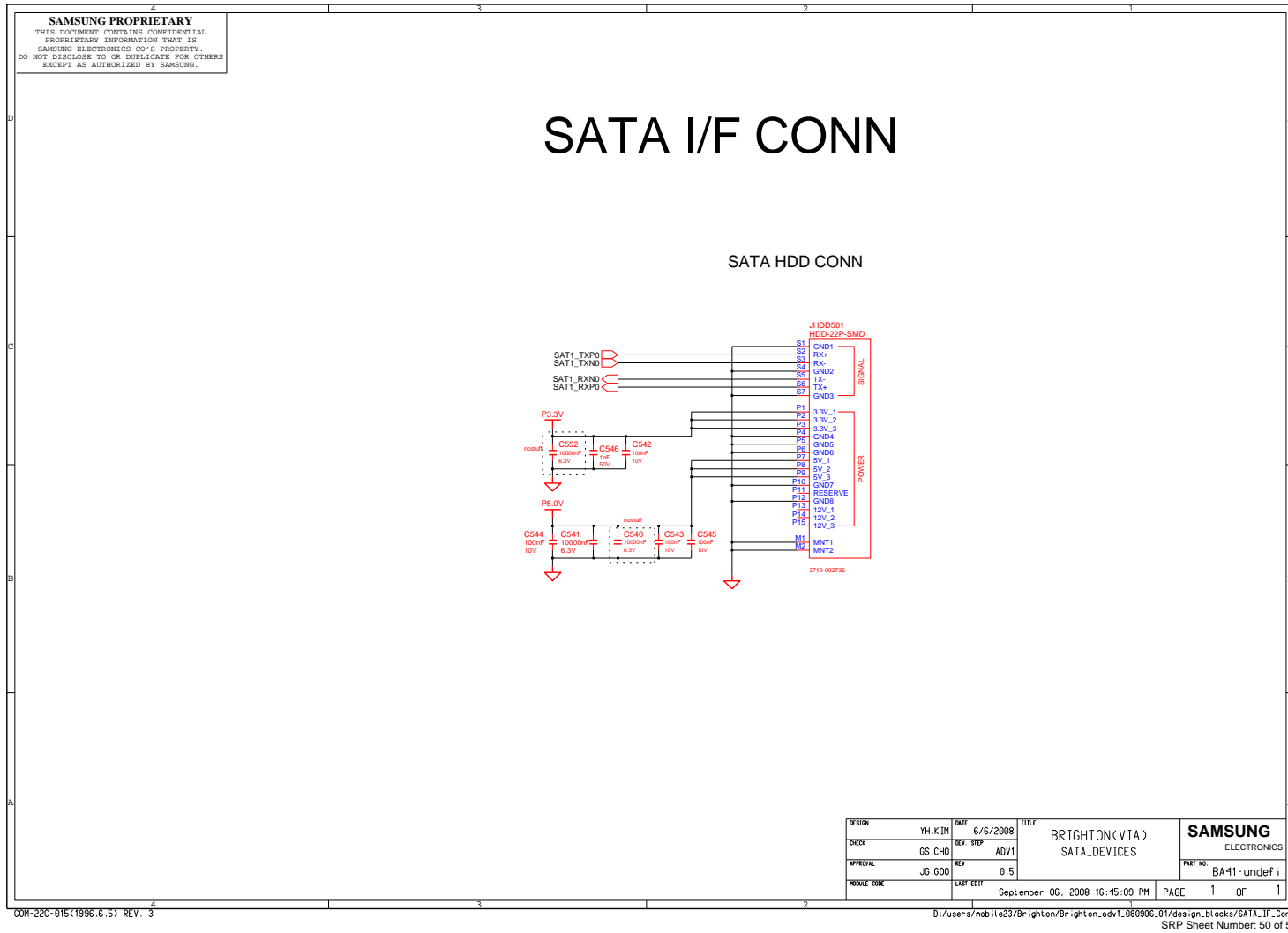
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